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A SIX-PORT MEASUREMENT DEVICE FOR HIGH POWER MICROWAVE VECTOR NETWORK ANALYSIS

Abstract

The changes experienced in technology due to the third industrial revolution have over the years contributed immensely to the development of efficient devices and systems. As a result, solutions have been provided to challenges encountered in the heating industry. However, higher efficiency and better performance has undoubtedly been highly sort after. This paper presents the complete industrial development of a new system of a microwave device for use in S-band networks (2.45 GHz ISM band in this application): a vector network analyzer (VNA). The VNA, which is designed based on the six-port measurement principle, provides accurate measurements of both magnitude and phase of the load reflection coefficient. The device is designed to have high power handling capabilities and works under the full operating conditions of high-power microwave generators. Initial measurements show that the device perform stable and can perform temperature-independent measurements over protracted periods. The system is suited for on-line monitoring and control of network parameters in industrial waveguide applications.

1. INTRODUCTION

Heating is arguably the commonest process in the manufacturing industry, where it is used to effect physical and chemical changes in raw materials to produce food, textile, and fuel, among others. However, industrial heating remains largely a sluggish, imprecise, and difficult process to control especially when done through conventional way of material surface heating. Microwave volumetric heating offers an exceptionally efficient solution to these problems. In this process, injected energy is transferred electromagnetically through the surfaces of workpieces, rather than as heat flux like in conventional methods. Infinitesimal elements in the workload volume are thus heated individually and at an approximately equal rate. Heating times and effective energy variation within workload are reduced significantly while maintaining competitive running costs. A basic industrial

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microwave heating system comprises a high-power magnetron-head that generates and supplies microwave energy at 900 MHz or 2.45 GHz to a cavity oven through a waveguide network. A typical transmission line features components such as an isolator for magnetron protection, an analyzer for network monitoring, and a tuner for maintaining maximum magnetron-load power coupling. Current high power microwave heating processes rely on the use of the loop coupler for measuring the reflection in waveguide networks. This device determines the reflection coefficient by measuring the forward and reverse power flowing in the guide section. However, the coupler only produces the magnitude of the reflection coefficient but not the phase. This measurement information is often inadequate to properly match the network.

In this paper, we present a simplified formulation for extracting the vector reflection from sampled wave-amplitude measurements in a microwave network. The discussed method is based on the six-port measurement technique first introduced in (Engen,1977), but without the need for extensive calibration. Using this formulation, we describe the design and implementation of a compact VNA capable of measuring the magnitude and phase of the reflection coefficient in high microwave power waveguide applications. It is useful in systems which require online and inline network parameter monitoring, where employing commercial VNAs may not be feasible. Empirical results show good performance when compared to a commercial VNA. The proposed VNA is designed for use in applications where the network is sourced by a 6-kW magnetron. Using simulations, the power handling capability of the VNA and its suitability for the intended application has been demonstrated. The presented VNA was designed as part of a larger system where reflection measurements are fed to another device which is used to achieve automatic tuning of the network in a feedback loop. Description of the tuning device is outside the scope of this paper and will not be discussed. However, references will be made to this device and its interface with the VNA.

This paper is organized as follows: Section 2 review some literature and section 3 discusses fundamentals of network analysis and the design of the network analyzer. Section 4 describes the implementation, calibration and evaluation of the developed system and section 5 concludes the paper.

2. LITERATURE REVIEW

There are many processes that take place in the manufacturing industries today. However, only few processes are indisputably integral to the continuous operation and success of these industries. Industrial heating by far has come a long way since its inception. It is employed in the industries to effect physical and chemical changes in raw materials for the fabrication of food (Sorică et al., 2021), medicines (Gartshore, Kidd & Joshi, 2021; Shah, 2019), textiles (Elshemy & Haggag, 2019; De-chao, 2015), fuels (MacDonald & Miadonye, 2018; Amornraksa & Sritangthung, 2020) and many more. Over the years, industrial heating has experienced advancements to improve upon the shortfalls of the conventional heating techniques. Microwave volumetric heating has provided an efficient solution to conventional heating methods as it heats both the core and surface of each element of the product simultaneously and approximately at equal rate. Information and data collected from this field has prompted a few studies aimed at developing microwave heating techniques with a

handful of prototypes developed. Traditional or conventional heating used in the early days of industrialization was achieved primarily through fuel-based heating techniques. In this method, the generated heat is transferred as heat flux to the surface of the product either by heat conduction, convection, radiation, or all three-transfer media. Physical and chemical changes take place from the surface to the core of the product and are dependent on certain properties like specific heat capacity and many more. Even though conventional heating system and equipment are easy to build, this heating techniques are not energy saving, time consuming, difficult to control heating flow rates, presents quality problems of products and raises CO_2 emission concerns.

As opposed to traditional heating method, electricity-based heating techniques have dynamically changed the heating mechanism to date. Although there are various electro-technologies employed for heating for instance induction and laser heating (Vishnuram et al., 2021; Caiazzo & Alfieri, 2018; Murzin, Kazanskiy & Stiglbrunner, 2021), the use of microwave energy has been indispensable. The use of microwave technology provides significant benefits such as energy efficiency, time saving, effective control of heat flow rate, improves CO_2 emissions and assures the quality level of products.

Microwave heating systems that exist have different designs. These differences primarily stem from the nature of the network analyzer and the tuner. In reference to the network analyzer which measures complex reflection coefficient characterizing the load, different design models exist based on the measurement principles employed. Wave separation method and Interference method are the categories under which network analyzers are made. Conventional network analyzers were designed based on wave separation methods. In this method, an incident wave injected into one network port is observed as responses at all ports and compared to stimulus. Reflection coefficient measurements are achieved provided the stimulus and back-propagating signal waves are separated since they appear at the same port. This separation is carried out using directional couplers or bridges which increases design cost. In contrast to wave separation method, interference method does not involve separation of port stimulus from responses. This method primarily depends on the combination of two waves to produce standing wave patterns along the transmission line. The creation and observation of the wave combinations can be achieved either simultaneously at different ports or sequentially at a given port. Six-port reflectometer typical operates on interference method. It is employed as the standard for complex measurement of the reflection coefficient of a device under test (DUT) using four power readings and can be easily calibrated for diverse applications (Moubarek & Gharsallah, 2016; Moubarek, Almanee & Gharsallah, 2019).

(Mohra, 2004) presented the design of a six-port reflectometer structure using two microstrip three-section couplers. In this design, the six-port reflectometer was developed on a Teflon substrate at a center frequency of 3.5GHz using dimensions of a three-section coupler. The **S** parameters which were simulated and measured were found around -20 dB with 2.0 dB maximum deviation. Reflections at the input port were also found to be less than -25dB. Although this design reduces the size of the reflectometer, the reflection coefficient was better as it is difficult to achieve perfection.

3. MATERIALS AND METHODS

3.1. Scattering parameters

In low frequency circuits, dimensions of circuit elements are small relative to the wavelength. Thus, these circuits can be analyzed as interconnections of active and lumped passive elements with unique currents and voltages at any point in the circuit. In such cases, phase delay between circuit nodes is negligible. Furthermore, since fields in low frequency circuit are supported by two or more conductors, the fields are considered transverse electromagnetic (***TEM***). This leads to quasi-static solutions to Maxwell's equations and the popular circuit theory concepts like Kirchhoff's laws etc. Although these basic concepts can be used to understand microwave analysis, they are not directly applicable to microwave circuits in general. This is especially true for non-***TEM*** lines such as waveguides, which support an additional set of fields: transverse electric (***TE***) and transverse magnetic (***TM***), whose voltages and currents cannot be uniquely defined.

In microwave circuits, signals are described by wave variables which are linked to waves physically traveling along transmission lines. As illustrated in Figure 1, variable describing waves impinging on a device's ports are denoted ***a*** whiles that of reflected and/or transmitted waves flowing outward are denoted ***b***. The magnitude of a wave variable is related to the mean power carried by its corresponding wave. The phase, however, is equal to the physical wave phase at a given reference plane.

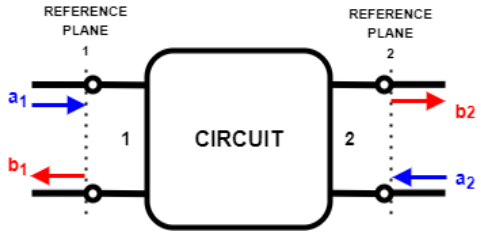

Fig. 1. A two port microwave circuit showing waves on its ports

Scattering (*S*) parameters provide an intuitive and complete description of a network at its ports. They unify the paradigm for direct measurement in ***TEM*** fields and the idea of incident, transmitted, and reflected waves. Consider an arbitrary ***n***-port microwave network with reference planes at each of its ports where the wave variables are defined. There are ***n*** impinging waves, $\boldsymbol{a_i}$ and ***n*** responses $\boldsymbol{b_j}$, where $i,j=1,\ldots n$. See Figure 2.

Here, the $\boldsymbol{n}^2$ transfer functions describing the response of port to stimuli are quantified by the ***S*** parameters $\boldsymbol{S_{ji}}$ given by Equation 1. The ***S*** parameters are classified into reflection coefficients $\Gamma_i = S_{ji}$ and transmission coefficients $S_{ii}, j \neq i$.

$$S_{ji} = \frac{b_j}{a_i},\ i,j = 1,\ldots n \tag{1}$$

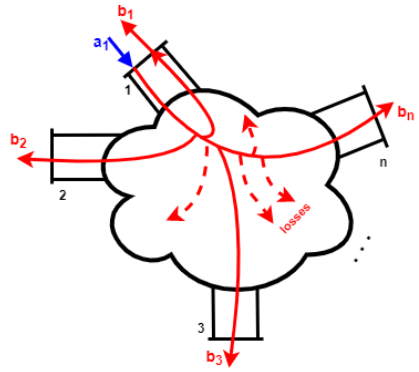

Fig. 2. Scattering of an impinging wave a_1 in an arbitrary *n*-port microwave network

3.2. Network Analyzer Technologies

The network analyzer is an instrument for measuring (complex) *S* parameters characterizing passive and active networks. There is different possible hardware configuration for the implementation of such an instrument. However, network analyzers can be categorized broadly based on the measurement principles employed: wave separation or interference.

3.3. Wave Separation Method

The wave separation method is conceptually straightforward, and the measurements are based directly on the ***S*** parameter definition (Equation 1). This method forms the working principle of almost all 'conventional' network analyzers available commercially. Here, an incident wave is injected into one network port and the responses at all ports are observed and compared to stimulus. To arrive at an ***S*** parameter, the phase difference, and amplitudes ratio of both the stimulus and the corresponding response must be determined. For reflection coefficient measurements, since the stimulus and back-propagating signal appear at the same port, the two waves must be separated. The functional overview of a conventional network analyzer is illustrated in Figure 3 with a 2-port device under test (DUT) connected and being measured.

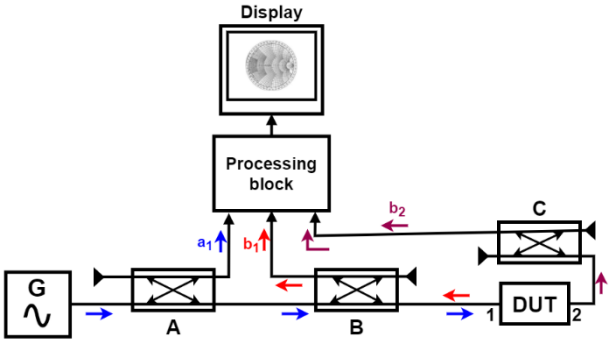

Fig. 3. Principal block diagram of a conventional network analyzer based on the wave separation method

The set-up uses three identical directional couplers or bridges, **A** for transmission and separation of stimuli and responses. The input signal supplied from the generator is delivered to the DUT through couplers **A** and **B** while a fraction of the stimulus is diverted to a processing unit. The reflected signal from the DUT and its output response are coupled to the processing unit through **B** and **C** respectively. In the processing unit, the wave amplitudes are extracted, and their respective ratios computed. The amplitude measurements are easily obtained using power detectors. On the other hand, estimation of the phase differences is achieved separately and can be quite complicated. To do this, most network analyzers employ heterodyne double-conversion receivers which are phase-locked to the incident wave.

3.4. Interference Method

Unlike the wave-separation method, the interference technique does not involve separating the port stimulus from the response. The method relies on the combination of the two waves to produce standing wave patterns along the transmission line. Several controlled linear combinations of the incident and reflected waves are setup in a measurement system and the resulting magnitudes are extracted. The creation and observation of the wave combinations can either be done simultaneously at various ports of the measurement system or achieved sequentially at a given port using multi-state hardware as is done in the slotted-line system (Miniature Linear Motion Series L12, 2019). With the observed scalar data, both magnitude and phase of the ***S*** parameters can be obtained.

3.5. The Six Port Reflectometer

The six-port reflectometer is a network analyzer based on the interference technique which measures the reflection coefficient of a connected device. The building block of the reflectometer is a linear six-port network. As illustrated in Figure 4, one port is connected to a signal source, another is terminated in a DUT, and the remaining four ports are connected to power detectors (D1–D4).

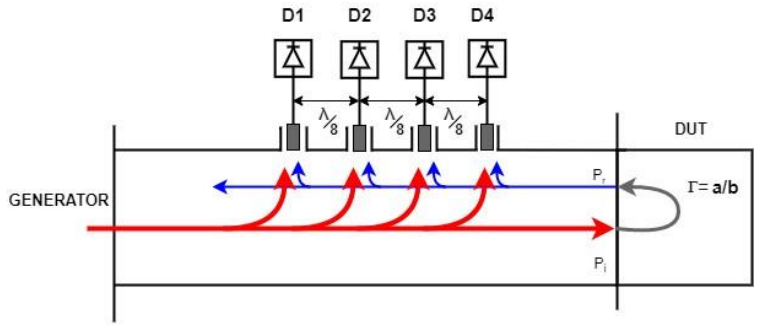

Fig. 4. Basic block diagram of the six-port reflectometer

The six-port device is described by a 6 × 6 scattering matrices relating its input and output power wave vectors, ***a*** and ***b***. Considering that the four ports 3–6 are connected to matched loads $\boldsymbol{a}_{3\text{-}6} = 0$, while Port 2 is connected to an unknown load characterized by a reflection

coefficient $\Gamma_L$to be retrieved i.e $a_2 = \Gamma_L b_2$. With the reciprocity of the device and symmetry across the guide cross section $(123 \leftrightarrow 456)$

$$[\boldsymbol{b}] = [\boldsymbol{S}]\begin{bmatrix} a_1 \\ \Gamma_L b_2 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{21} \\ S_{21} & S_{11} \\ S_{31} & S_{61} \\ S_{41} & S_{51} \\ S_{51} & S_{41} \\ S_{61} & S_{31} \end{bmatrix}\begin{bmatrix} a_1 \\ \Gamma_L b_2 \end{bmatrix} = \begin{bmatrix} S_{11} + \Gamma_L^{'} S_{21} \\ \Gamma_L^{'}/\Gamma_L \\ S_{31} + \Gamma_L^{'} S_{61} \\ S_{41} + \Gamma_L^{'} S_{51} \\ S_{51} + \Gamma_L^{'} S_{41} \\ S_{61} + \Gamma_L^{'} S_{31} \end{bmatrix} a_1 \tag{2}$$

with

$$\Gamma_L^{'} = \frac{S_{21}\Gamma_L}{1 - S_{11}\Gamma_L} \tag{3}$$

The power measured at the 4 power ports are

$$\begin{bmatrix} |b_3|^2 \\ |b_4|^2 \\ |b_5|^2 \\ |b_6|^2 \end{bmatrix} = \begin{bmatrix} \left|s_{31} + \Gamma_L^{'} s_{61}\right|^2 \\ \left|s_{41} + \Gamma_L^{'} s_{51}\right|^2 \\ \left|s_{51} + \Gamma_L^{'} s_{41}\right|^2 \\ \left|s_{61} + \Gamma_L^{'} s_{31}\right|^2 \end{bmatrix} |a_1|^2 =$$

$$= \begin{bmatrix} |s_{31}|^2 + |s_{61}|^2\left|\Gamma_L^{'}\right|^2 + 2|s_{31}||s_{61}|\left|\Gamma_L^{'}\right| cos\left(\angle\Gamma_L^{'} + \angle s_{61} - \angle s_{31}\right) \\ |s_{41}|^2 + |s_{51}|^2\left|\Gamma_L^{'}\right|^2 + 2|s_{41}||s_{51}|\left|\Gamma_L^{'}\right| cos\left(\angle\Gamma_L^{'} + \angle s_{51} - \angle s_{41}\right) \\ |s_{51}|^2 + |s_{41}|^2\left|\Gamma_L^{'}\right|^2 + 2|s_{51}||s_{41}|\left|\Gamma_L^{'}\right| cos\left(\angle\Gamma_L^{'} + \angle s_{41} - \angle s_{51}\right) \\ |s_{61}|^2 + |s_{31}|^2\left|\Gamma_L^{'}\right|^2 + 2|s_{61}||s_{31}|\left|\Gamma_L^{'}\right| cos\left(\angle\Gamma_L^{'} + \angle s_{31} - \angle s_{61}\right) \end{bmatrix} |a_1|^2 \tag{4}$$

The phases of the four probes depend on their positions. If the four probes are spaced by $d = \lambda_g/8$ and are assumed to have the same coupling level $|s_{31}| = |s_{41}| = |s_{51}| = |s_{61}| = C$ then,

$$\begin{bmatrix} s_{31} \\ s_{41} \\ s_{51} \\ s_{61} \end{bmatrix} = \begin{bmatrix} Ce^{j\frac{3kd}{2}} \\ Ce^{j\frac{kd}{2}} \\ Ce^{-j\frac{kd}{2}} \\ Ce^{-j\frac{3kd}{2}} \end{bmatrix} = \begin{bmatrix} Ce^{j\frac{3\pi}{8}} \\ Ce^{j\frac{\pi}{8}} \\ Ce^{-j\frac{\pi}{8}} \\ Ce^{-j\frac{3\pi}{8}} \end{bmatrix} \tag{5}$$

and

$$\begin{bmatrix} |b_3|^2 \\ |b_4|^2 \\ |b_5|^2 \\ |b_6|^2 \end{bmatrix} = C^2 \begin{bmatrix} 1 + \left|\Gamma_L^{'}\right|^2 + \sqrt{2}\left|\Gamma_L^{'}\right|\left[-cos\left(\angle\Gamma_L^{'}\right) + sin\left(\angle\Gamma_L^{'}\right)\right] \\ 1 + \left|\Gamma_L^{'}\right|^2 + \sqrt{2}\left|\Gamma_L^{'}\right|\left[cos\left(\angle\Gamma_L^{'}\right) + sin\left(\angle\Gamma_L^{'}\right)\right] \\ 1 + \left|\Gamma_L^{'}\right|^2 + \sqrt{2}\left|\Gamma_L^{'}\right|\left[cos\left(\angle\Gamma_L^{'}\right) - sin\left(\angle\Gamma_L^{'}\right)\right] \\ 1 + \left|\Gamma_L^{'}\right|^2 + \sqrt{2}\left|\Gamma_L^{'}\right|\left[-cos\left(\angle\Gamma_L^{'}\right) - sin\left(\angle\Gamma_L^{'}\right)\right] \end{bmatrix} |a_1|^2 \tag{6}$$

where $\lambda_g$is the guide wavelength.

Combining the matrix row equations

$$-|b_3|^2 + |b_4|^2 = |b_5|^2 - |b_6|^2 = 2\sqrt{2}C^2\left|\Gamma_L^{'}\right| cos\left(\angle\Gamma_L^{'}\right)|a_1|^2 \quad (7)$$

$$|b_3|^2 - |b_6|^2 = |b_4|^2 - |b_5|^2 = 2\sqrt{2}C^2\left|\Gamma_L^{'}\right| sin\left(\angle\Gamma_L^{'}\right)|a_1|^2 \quad (8)$$

$$|b_3|^2 + |b_5|^2 = |b_4|^2 + |b_6|^2 = 2C^2\left(1 + \left|\Gamma_L^{'}\right|^2\right)|a_1|^2 \quad (9)$$

From Equations 7 and

$$\sqrt{(-|b_3|^2 + |b_4|^2 + |b_5|^2 - |b_6|^2)^2 + (|b_3|^2 - |b_6|^2 + |b_4|^2 - |b_5|^2)^2} = 4\sqrt{2}C^2\left|\Gamma_L^{'}\right||a_1|^2 \quad (10)$$

$$\sqrt{(-|b_3|^2 + |b_5|^2 + |b_4|^2 - |b_6|^2)^2 + (|b_3|^2 - |b_5|^2 + |b_4|^2 - |b_6|^2)^2} = 4\sqrt{2}C^2\left|\Gamma_L^{'}\right||a_1|^2 \quad (11)$$

From Equations 9, 10, and 11

$$|b_3|^2 + |b_5|^2 + |b_4|^2 - |b_6|^2 = 4C^2\left(1 + \left|\Gamma_L^{'}\right|^2\right)|a_1|^2 \quad (12)$$

$$\sqrt{(|b_3|^2 - |b_5|^2)^2 + (|b_4|^2 - |b_6|^2)^2} = 4C^2\left|\Gamma_L^{'}\right||a_1|^2 \quad (13)$$

then

$$\left|\Gamma_L^{'}\right|^2 - \frac{|b_3|^2+|b_4|^2+|b_5|^2+|b_6|^2}{\sqrt{(|b_3|^2-|b_5|^2)^2+(|b_4|^2-|b_6|^2)^2}}\left|\Gamma_L^{'}\right| + 1 = 0 \quad (14)$$

or

$$X = \frac{|b_3|^2+|b_4|^2+|b_5|^2+|b_6|^2}{\sqrt{(|b_3|^2-|b_5|^2)^2+(|b_4|^2-|b_6|^2)^2}} = \frac{\left|\Gamma_L^{'}\right|^2+1}{2\left|\Gamma_L^{'}\right|} = \frac{e^{-ln\left|\Gamma_L^{'}\right|}+e^{ln\left|\Gamma_L^{'}\right|}}{2} = cos(\,ln\left|\Gamma_L^{'}\right|)\,. \quad (15)$$

Therefore, from Equations 14 and 15, the modulus of $\Gamma_L^{'}$is obtained as follows

$$\left|\Gamma_L^{'}\right| = X + \sqrt{X^2 - 1} = e^{cosh^{-1}(X)} \quad (16)$$

The phase of $\Gamma_L^{'}$ is then obtained using Equations 2.7 and 2.8

$$\angle\Gamma^{'} = atan2[(|b_3|^2 + |b_4|^2 - |b_5|^2 - |b_6|^2), (-|b_3|^2 + |b_4|^2 + |b_5|^2 - |b_6|^2)] \quad (17)$$

Finally, inverting Equation 2.3, the reflection coefficient characterizing the load is given by

$$\Gamma_L = \frac{\Gamma_{L_L}^{'}}{S_{11}\Gamma_{L_L}^{'}+S_{21}} \quad (18)$$

3.6. Reflectometer Model

The reflectometer block was modeled as a 100 mm WR340 guide section with four SMA probes inserted into its broadface, $\frac{\lambda_g}{8}$ apart and symmetrical across the block's vertical cross-section (Figure 5).

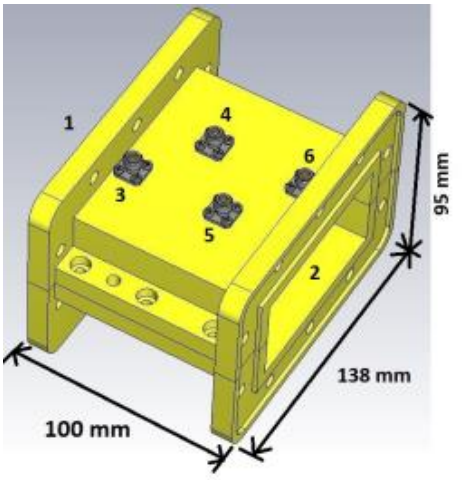

Fig. 5. Reflectometer block

To control the coupling level of the ports, each probe was trimmed such that their tip was 2.7 mm from the inner guide wall. The probes were then shifted 15 mm away from the longitudinal guide axis to further reduce the coupling. This was to ensure that only a small amount of power is coupled and that the probe did not heavily perturb the waves in the guide. From simulation in CST MWS, each probes registered a $\Gamma_L^{'} - 78.7$ dB coupling level across the S-band. The reflectometer block was also realized from aluminum. Measurement of the four ports with the Agilent E5071c VNA showed that each port experienced higher coupling levels with approximately -60 dB at 2.45 GHz (Figure 6).

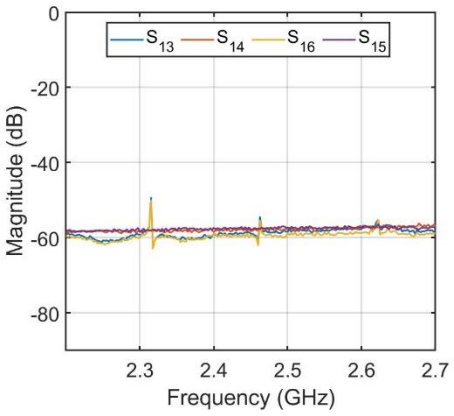

Fig. 6. Measured coupling coefficient magnitudes of the 4 probes

This was due to probe trimming error. This will be corrected in future work towards high power measurements. However, for low power measurements, the high port coupling levels are within safe levels for the device. The most important thing, which was satisfied, was that all four ports had approximately the same measured levels. This is an important premise for the reflectometer's operation (see Equations 5 and 6).

3.7. VNA Front-End

The flow of coupled power waves through the functional blocks of the VNA front-end is summarized in Figure 7.

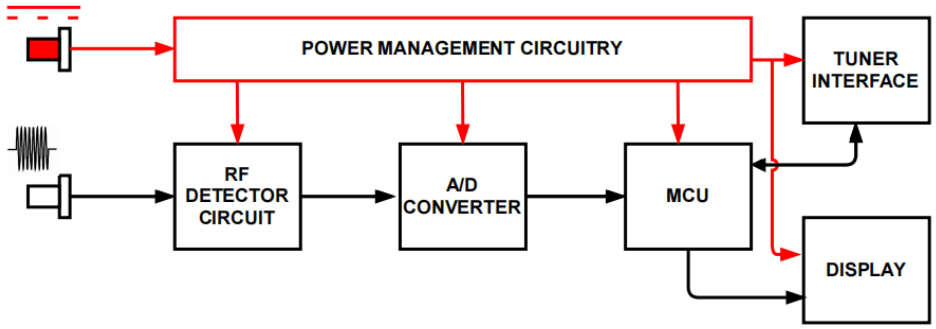

Fig. 7. Function block diagram of the VNA front end

Power coupled from the waveguide is measured by an RF detector circuit. The analog output of the detector circuit is fed to an analog-to-digital converter (ADC) which produces digital codes representing the measured power. The digitized measurements are processed by a microcontroller unit (MCU) to retrieve the data about reflection in the waveguide network. Reflection measurements are also shown on a display. The front end is powered by a DC supply. A power circuitry manages power quality and distributes appropriate portions to all the functional blocks.

3.8. RF Detector Circuit

The detector circuit measures RF power coupled from each reflectometer port. The circuit uses the Analog Devices' AD8318 demodulating logarithmic amplifier as its primary element. AD8318 converts RF input signals to corresponding low noise dB-scaled voltage outputs by employing a successive fast response compression technique over a chain of nine amplifier stages, each of which is equipped with a detector cell (Figure 8 a and b).

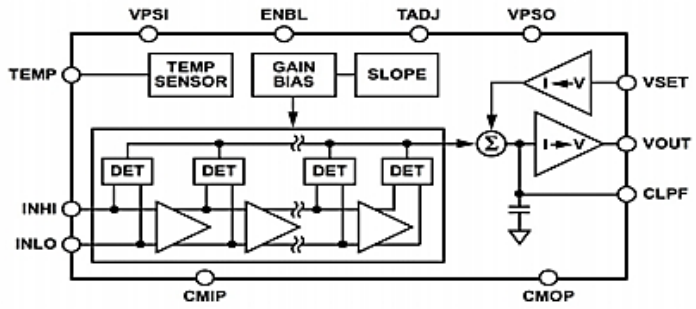

Fig. 8a. Functional Block Schematic

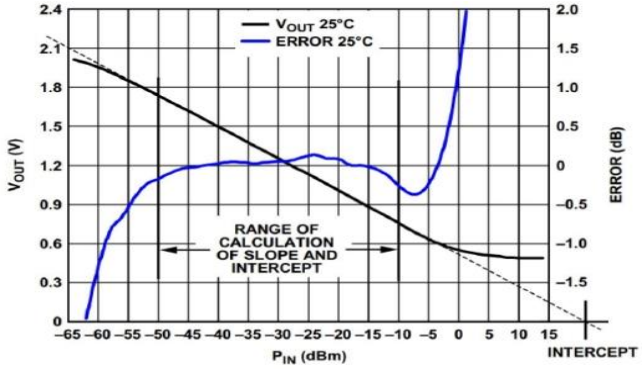

Fig. 8b. Typical response vs. input signal amplitude

The device has an impressive 60 dB usable input dynamic range with a high degree of log conformance over the range (error = ±1 dB). Typical device output voltage temperature stability is ±0.5 dB. Additional device information can be found in (Practical Design Techniques for Sensor Signal Conditioning, 2019). To configure the AD8318 for measurement, a portion α of the output voltage is feedback to the device's setpoint interface by connecting the $\boldsymbol{V_{OUT}}$ pin to the $\boldsymbol{V_{SET}}$ pin directly or through a ground referenced resistive feedback divider. This yields an output which is a decreasing linear-in-dB function of input RF signal power $\boldsymbol{P_{IN}}$. A direct $\boldsymbol{V_{OUT}}$-$\boldsymbol{V_{SET}}$ connection maintains the chip's nominal logarithmic slope (typically -24 mV/dB with $\boldsymbol{P_{INTERCEPT}}$ = 20 dBm intercept on the abscissa) whiles introducing divided feedback allows for shaping the chip's response function and output dynamics. ***Slope*** is scaled by the feedback factor α. The increase in ***Slope*** reduces dynamic range which is, of course, limited to the swing capability of AD8318's PNP output stage: $\boldsymbol{\alpha V_{OFFSET} < V_{OUT} < (V_{PS} - 0.4V)}$ where $\boldsymbol{V_{OFFSET}}$ = 0.5 V and $\boldsymbol{V_{PS}} \in$ [4.5 V–5.5 V] are the detector's output offset and appropriately decoupled positive supply respectively (Practical Design Techniques for Sensor Signal Conditioning, 2019). In this work, the direct output setpoint connection was employed as the corresponding $\boldsymbol{V_{OUT}}$ range matches the full-scale range of the analog-to-digital converter (ADC) in the next stage. Furthermore, this choice also eliminated possible output drifts due to temperature variations that may occur in the resistive feedback elements. To trim temperature drift of the AD8318 functionality,

a ground referenced RTADJ resistor is used. For optimal temperature compensation in the S-band, RTADJ was set as 499Ω (1 MHz to 8 GHz, 70 dB Logarithmic Detector/Controller, 2019). The CMIP and CMOP I/O common pins were also connected to a low impedance ground plane for optimum electrical and thermal performance.

The single-ended RF input to the detector and input stage common (INLO) were ac-coupled with two 220 pF capacitors. The capacitor pair, together with an internal 10 pF capacitor, formed a high pass corner at ~ 16 MHz which cuts out unwanted lower frequency signals particularly the spurious digital noise from the front-end's clocking system. The impedance of the input interface was estimated as 27 – j75Ω at 2.45 GHz. While the input could have been reactively matched, it was not necessary. A 52.3Ω resistor was used to shunt the feed line. This terminating resistor combined with the relatively high input impedance of the chip provide a wideband 50Ω match. Each reflectometer probe couples -78.7 dB of the 6-kW output power launched by the microwave generator in the target application. This means approximately -11 dBm of power will be fed into the detector circuit. A fixed resistor RF attenuator was introduced at the circuit's input to put its operation in the middle of the AD8318's linear response and low error range. Furthermore, it would protect the AD8318 chip (12 dBm input power rating) in events of microwave power spikes which may result from magnetron malfunction, heavy network reflection, or arcing. The ***T*** structure, referenced to $\boldsymbol{Z_0}$ = 50Ω, produced a wideband 19.28 dB attenuation with an 87 dB return loss. The series and shunt resistances were related to the voltage ratio ***N*** by Equations 19 and 20 respectively.

$$R_5 = R_6 = Z_0\left(\frac{N-1}{N-1}\right) \tag{19}$$

$$R_7 = Z_0\left(\frac{2N}{N^2-1}\right) \tag{20}$$

Effects of the attenuator were compensated for during device calibration. Finally, a grounded 100 nF capacitor was connected the CLPF pin to reduce the output video bandwidth and hence smoothen the detector output while maintaining an adequate slew rate. The RF detector circuit with the resistor attenuator is shown in Figure 9.

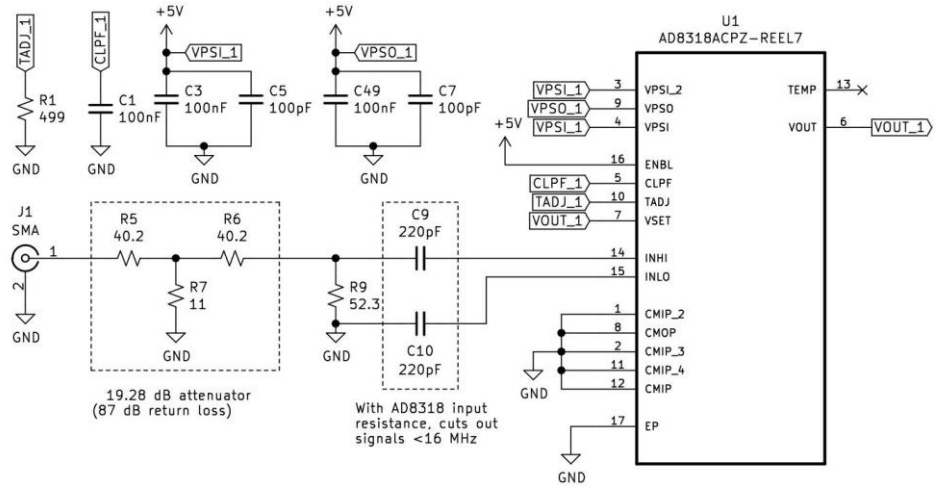

Fig. 9. RF detection circuit with signal attenuator for a reflectometer port

3.9. ADC and Logic Level Translators

The detector outputs of the four ports were interfaced with the Texas Instruments (TI) ADS7841 precision sampling ADC as shown in Figure 10.

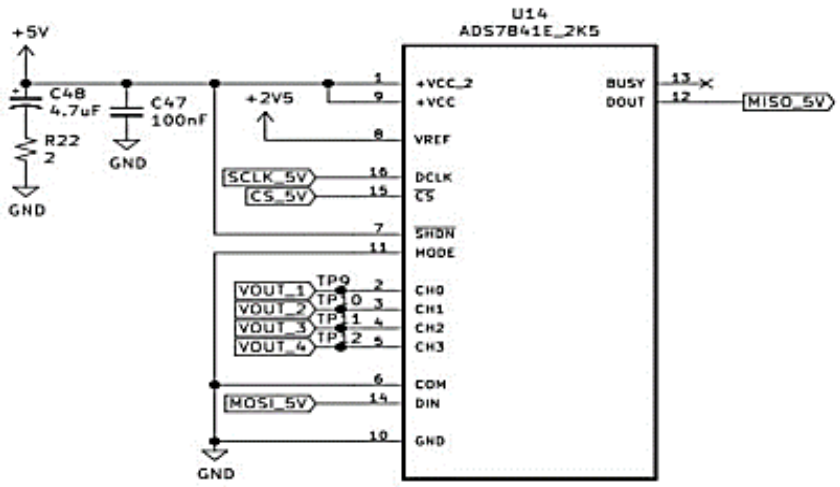

Fig. 10. ADS7841 based circuit for digitizing RF detector output voltages

The ADS7841 is a 4-channel successive-approximation register (SAR) ADC with a 200 kHz max throughput and a programmable resolution: 8 or 12 bits. The ADC was configured in 12-bit mode and its voltage reference V_{REF} was provided externally by an Analog Devices' ADR421 2.5 V ultra-precision reference (± 0.04% tolerance, 3-ppm/°C temperature coefficient) (Ultraprecision, Low Noise, 2.048 V/ 2.500 V/ 3.00 V/ 5.00 V XFET ® Voltage References, 2013). The four analog measurements on the single-ended channels were sequentially captured ADC by the ADC's input multiplexer in the hold mode. The configuration of the analog multiplexer was set by conversion control bytes provided via the DIN (MOSI) pin by the MCU through its 8-bit serial peripheral interface (SPI) bus. The ADS7842 requires an external clock to run the conversion process. A 125 kHz clock signal was supplied by the external processor via the DCLK (SCLK) pin. Data on the MOSI line was latched on the rising edge of DCLK. The communication between the converter and the MCU consists of eight clock cycles. Each complete conversion was accomplished with three serial communications (Figure 11).

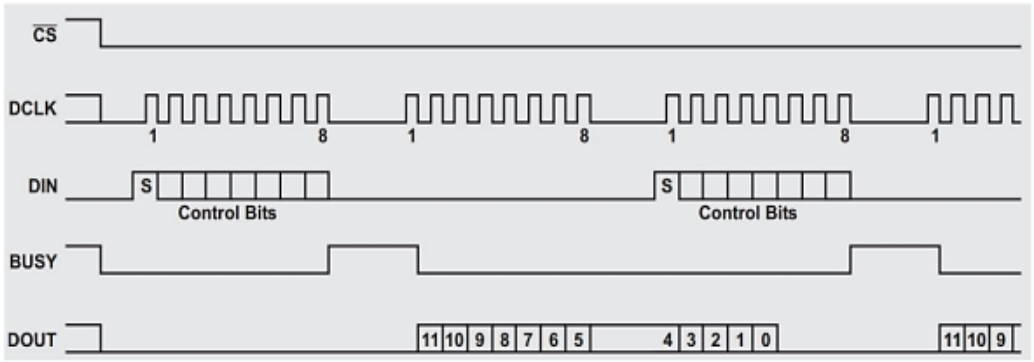

Fig. 11. Timing diagram of the ADS7841's 24-clock cycle per conversion, 8-bit SPI interface

The digital output is shifted out of the DOUT (MISO) pin on the falling edge of DCLK. The three conversion results are manipulated in the MCU to extract the 12-bit measurement word. The ADS7841 was powered by a +5 V rail whiles the interfacing MCU operated on +3.3 V. As such they have different I/O logic-level standards. To resolve the voltage incompatibilities between the two parts and ensure proper operation of the system, logic translators were used on the data bus. The MOSI and SCLK lines were run through the TI SN74LVC2T45 dual-bit bus transceiver whiles the MISO line was connected to the SN74LVC1T45 transceiver. The translators supported bidirectional logic-level shifting and hence required two separate power-supply rails: +3.3 V and +5 V. However, since the individual SPI lines were unidirectional, translation directions were 'locked' to one sense by tying the chips' DIR pins to ground as shown in Figure 12.

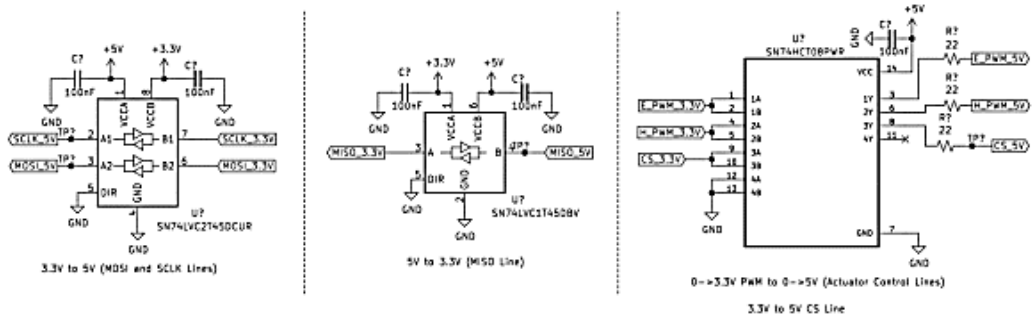

Fig. 12. Logic Level Translators

For the SPI chip select (CS) line, the unidirectional SN74HCT08 AND gate chip was used for level shifting. All transceivers had data rates upwards of 1 Mbps, which was more than enough for the ADS7871-MCU communication. Furthermore, the logic translators acted as buffer registers which acted as a Faraday shield between the converter's digital lines and the data bus thus to minimizing loading on the ADC's digital output (Practical Design Techniques for Sensor Signal Conditioning, 1999). This was very useful even though the ADS7841 has tri-state I/Os.

All power supplies to ADC, reference, and level-shifters were well bypassed with 100 nF capacitors to filter out noise originating from nearby digital logic and switching power supplies. Additional 4.7 μF and 2Ω series resistor was added to the ADC rail to improve the noise suppression. This was particularly important because the ADS7841's basic SAR architecture is very sensitive to glitches on the power supply, reference, and digital inputs latching onto the analog comparator. Furthermore, the ADC has no inherent noise rejection scheme on the $\boldsymbol{V_{REF}}$ input (12-Bit, 4-Channel Serial Output Sampling Analog-to-Digital Converter, 2001). The reference input to the ADC was bypassed using a 100nF capacitor. The decoupling also safeguarded the ADC performance under fast transient loading.

3.10. MCU and Peripheral Interfaces

The digitized measurement signals from the ADS7841 were processed by the STM32F334K8 mixed signal MCU running at 8 MHz. The MCU clock was sourced from a high-speed internal (HSI) RC oscillator, allowing for a simplified design with fairly accurate system and peripheral operation. The MCU also features an embedded floating-point unit (FPU) for supporting fast and reliable precision computations. Control and reading of the external ADC was achieved via the full-duplex 125 kbps SPI interface with the MCU set-up as master. The SPI communication was set up in MODE 0 (CPOL=0, CPHA=0) to support the digital interface of the ADS7841.

The waveguide network parameters were then computed from the four measured power magnitudes following Equations 16, 17 and 18. The parameters were displayed on a 16x2 character LCD, which was operated in 4-bit mode and controlled by the MCU via its standard 100 kHz inter-integrated circuit (I^2C) communication interface. The I^2C interface and the LCD's 16-pin parallel-port were connected via TI's PCF8574 8-bit I/O expander (Figure 13).

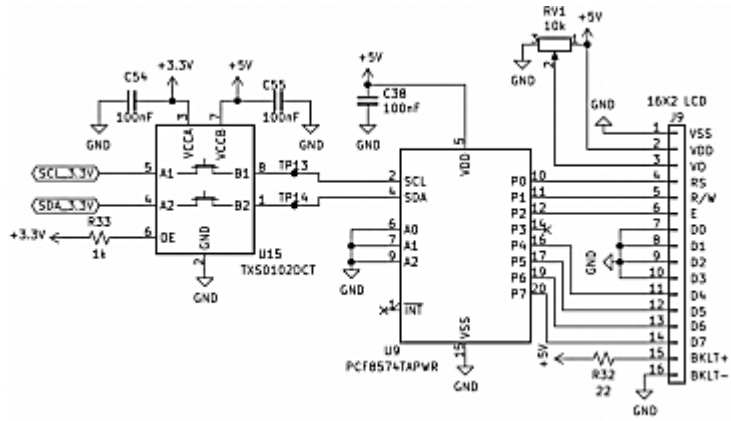

Fig. 13. The PCF8574 8-bit IO expander, TXS0102 translator and LCD interface

Like the SPI case, the serial clock (SCL) and serial data (SDA) I^2C lines were level shifted using the TI TXS0102 bidirectional auto direction-sensing translator. The dual-supply level translator, which employs a pass-gate architecture, has internal 10 kW pull-up resistors on its I/Os to adequately support the open drain drivers on the I/O pins of the MCU and PCF8574 (Remote 8-Bit I/O Expander for I2C Bus, 2015; Arm®Cortex®-M4 32b MCU+FPU,

(STM32F334x4 STM32F334x6 STM32F334x8). Datasheet, 2020). Therefore, no external pull-up was required. TXS0102 also features an output one-shot edge-rate accelerator circuitry to handle fast rising signal in the I^2C communication and to improve the current drive capability of the I/O driver (2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications, 2018). All address inputs A [0...2] of the PCF8574 were tied to ground, setting its address as 0×70. The +6 V powered actuator features an integrated self-configurable digital position controller composed of a factory-programmed Microchip PIC12F617 MCU and a ROHM BA6417F reversible motor driver. The actuator was controlled using a single 5V 1 kHz pulse-width modulation (PWM) signal whose duty cycle corresponded to the desired position expressed as a percentage of full stroke extension. The device also had built-in linear potentiometer which provided a feedback signal with a 0 - 3.3 V scaled amplitude proportional to the rod position with respect to the full stroke. Therefore, each of the two actuator interfaces had 4 pins: +6V, GND, PWM, and feedback. The PWM control signals were generated by STM32F334K8's high-resolution general-purpose timers and level-shifted to 0–5 V by the SN74HCT08 chip, to access the full stroke range of the actuator. 22 Ω resistors were placed on each PWM line post translation. This is very important to reduce dynamic switching currents. A typical CMOS gate (SN74HCT08) combined with PCB trace and (eventual) through-hole interface will create approximate 10 pF load (Practical Design Techniques for Sensor Signal Conditioning, 1999). In the absence of an isolation resistor, the SN74HCT08's 0.1 V/ns logic output slew rate produces about 100 μA dynamic current. Furthermore, all unused input pins are grounded as floating inputs could lead to slower input edge rates, which when coupled with noise generated on the power rails when the output switches, can cause excessive ringing and output errors (Implications of Slow or Floating CMOS Inputs, 2016). The actuator feedback signals were digitized by the MCU's built-in 12-bit ADC running at 2 MHz. The ADC has only one output data register serving all channels and it can digitize only one analog input at a time. The two signals could be digitized with single conversions interleaved with output register reading and ADC re-initialization (with a different analog channel). However, this wastes CPU resources and makes the tuner control error prone due to delays. An efficient solution was to scan the two channels. Here, a sequencer is employed at the ADC input to schedule the conversions and then link the output data register to the MCU's random access memory (RAM) using the direct access memory (DMA) controller.

The MCU was powered by a +3.3 V supply with 100 nF decoupling capacitor per VDD pin plus a 4.7 μF bulk capacitor. The analog reference (VDDA) of the MCU was also supplied separately with a +3.3 V rail but with additional filtering to eliminate high frequency crosstalk between the MCU's analog and digital domains. This is particularly important in this case because the MCU's HSI oscillator serves as the clock source for the whole front-end. For instance, phase noise on SCLK signal raises the distortion and noise floor thus degrading the ADS7841's signal-to-noise ratio. To prevent this, it is essential to keep the clock jitter comparable to the ADC's aperture jitter. The analog supply filter was formed from a series ferrite bead and the high *Q* 100 nF bypass capacitor (Figure 14).

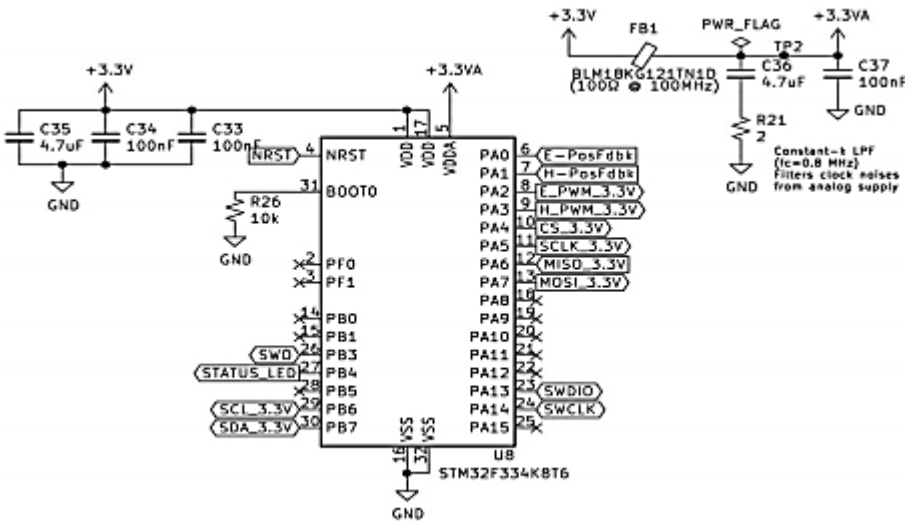

Fig. 14. The STM3232F334K8 MCU

The low-pass filter network was damped with a 2Ω resistor and 4.7μF series bulk capacitor to reduce possible resonance peaking without degrading the effectiveness of the bypass. Resonance peaking may occur since the resonant frequency of the undamped network is below the crossover frequency of the bead (~80 MHz) (BLM18KG121TN1D: Chip Ferrite Bead, 2020).

The MCU was then fitted with a 6-pin serial wire debug (SWD) interface for in-circuit programming and debugging via the ST-LINK probe. To prevent parasitic MCU resets, the NRST pin of the SWD interface was loaded with a 100nF debouncing capacitor. The BOOT0 pin was grounded through a 10 kΩ to allow activation of the bootloader during programming. A status light emitting diode (LED) was added for signaling.

3.11. Power Supply

The front-end was a mixed-voltage system that required +3.3 V, +5 V, and +6 V for the various on-board supplies as shown in Figure 15.

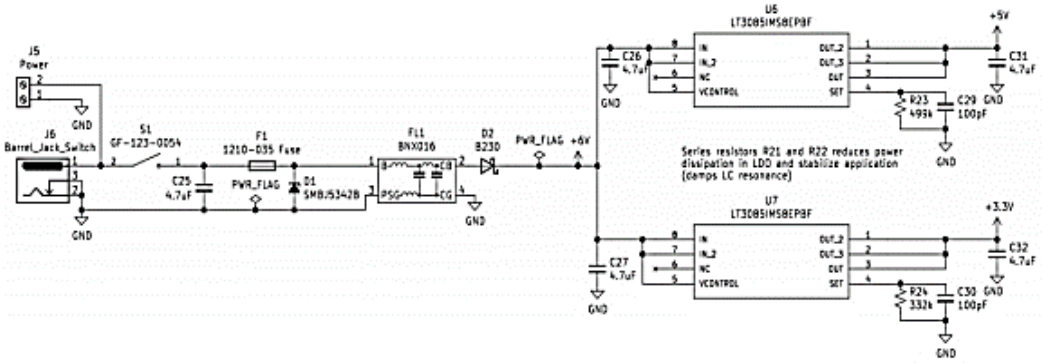

Fig. 15. Power Management Circuitry

Power was sourced from a +6V DC supply barrel jack or screw terminal and a SPST switch. The supply voltage is smoothed with a 4.7 μF capacitor to remove supply ripples. A resettable PPTC fuse (+6 V, hold = 0.3 A, trip = 0.7 A) and Zener diode (+6.8 V, 5W) were introduced for overcurrent and overvoltage protection respectively. The fuse rating allowed for the DC power circuit to support the actuators even under stalling conditions (maximum 0.46 mA stall current). For reliable attenuation of power line noises due to EM interference, a BNX016 EMI suppression filter was installed. A series Schottky barrier diode was then fitted for reverse polarity protection. Two Analog Devices' LT3085 adjustable 500 mA low dropout (LDO) linear regulators were employed to derive +5 V and +3.3 V supplies from the +6 V main line using single 499kΩ and 322kΩ voltage setting resistors, $\boldsymbol{R_{SET}}$ respectively. Ground-referenced 100pF capacitors were connected across $\boldsymbol{R_{SET}}$ to bypass the $\boldsymbol{R_{SET}}$'s shot noise and the LDO's reference current noise. 4.7μF low ESR capacitors were connected at the LT3085 inputs and outputs for decoupling and regulation stability.

4. RESULTS AND DISCUSSIONS

4.1. Prototype 1

A first working prototype of the network analyzer was built using off-the-shelf components for reflectometer's read-out circuit. The prototype, shown in Figure 16, had AD8318-based detector breakout circuit boards connected to the reflectometer's ports.

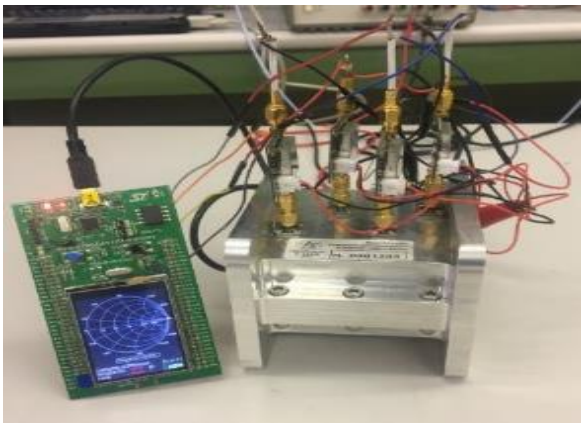

Fig. 16. First working prototype of the vector network analyzer

The analog DC outputs of each detector was fed to ADC inputs of STM32F429 evaluation board (based on the STM32F429ZIT6 MCU running at 180 MHz) and converted with the assistance of the DMA controller. The computed reflection coefficient was displayed graphically on the board's QVGA TFT LCD display. The analyzer prototype was calibrated based on the method in above and was tested. Although, it produces fairly accurate measurements, it was plagued with spurious errors which were attributed to the parasitic noise in the setup's poor cabling.

4.2. Prototype 2

Based on the fair results obtained from the first VNA prototype, a second was built for more accurate and stable measurements. The detector readout circuit as well as a closed-loop tuner control interface was designed and assembled on a printed circuit board (PCB).

4.3. PCB Design

The schematic of the front-end was captured and laid out using the KiCad EDA software. The PCB was designed with a 4-layer stack-up having separate planes dedicated to power, ground, and signals. The stack-up from top to bottom was: signal, ground, power, and signal. The stack-up was very important to proper performance of critical circuitry of the mixed-signal front-end. Placing the internal power and ground planes adjacent to each other provided additional inter-plane capacitance which improved high frequency decoupling of the power supply. The power plane is split to accommodate the three supply voltages whereas the ground plane is left uninterrupted. The large internal ground plane provided a low impedance return path for decoupling high frequency currents caused by fast digital logic but also minimizes EMI emissions. The ground plane also acted as a shield where sensitive signals cross. The board was sectioned into power, RF, analog, and digital areas with proper isolation practices to prevent the different signals from interfering with each other. Additionally, the RF frontend are adequately sectioned off vertically across all layers except the ground layer. Ground pours were made on top and bottom layers and connected to internal ground plane using multiple vias for improved thermal and electrical performances of the board. The power management circuitry was laid-out near the edges of the board to improve thermal performance of the LDOs. All power and ground pins of integrated circuits (ICs) were connected directly to the respective internal planes through vias and with short traces to avoid excessive loading. Decoupling capacitors were laid very close to the corresponding IC power pins and terminated through vias to the internal ground plane to preserve bypass effectiveness. 50Ω controlled impedance traces were used at the RF detector inputs to connect corresponding SMA connectors for good matching. Other essential signal routing, decoupling, and grounding techniques were observed to optimize PCB layout and maintain signal integrity. Test points have been placed on the signal and power lines for debugging and troubleshooting purposes. 3D renders of the designed board are shown in Figure 17.

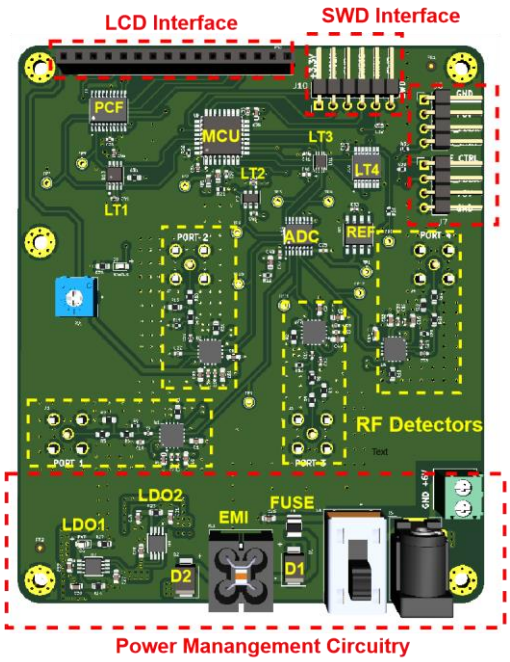

Fig. 17. VNA front-end

4.4. Calibration of proposed VNA

A simple two-point board-level calibration process was performed on each port to accurately obtain the transfer characteristics of the corresponding RF detector circuit at 2.45 GHz. This is because the slope and intercept $\boldsymbol{P_{INTERCEPT}}$ vary from one AD8318 device to another. Furthermore, since the exact attenuation produced by the realized fixed resistor pad is not easy to quantify, each attenuator and its associated AD8318 chip was calibrated together as a unit. The output voltage of the RF detector circuit in response to a power input $\boldsymbol{P_{IN}}$ can be expressed as

$$V_{OUT} = Slope \times (P_{IN} - P_{INTERCEPT}) \tag{21}$$

The calibration involved applying two known signal levels $\boldsymbol{P_{IN1}}$ and $\boldsymbol{P_{IN2}}$ to the detector circuit and measuring the corresponding output voltages $\boldsymbol{V_{OUT1}}$ and $\boldsymbol{V_{OUT2}}$. $\boldsymbol{P_{IN1}}$ and $\boldsymbol{P_{IN2}}$ were chosen from the linear-in-dB operating range of the AD8318 chip. The slope and intercept of the circuit transfer function were obtained from Equations ii and iii. ***Slope*** and $\boldsymbol{P_{INTERCEPT}}$ were stored in the device memory and are used in Equation iv to obtain the value of an unknown $\boldsymbol{P_{IN}}$ based on the measured $\boldsymbol{V_{OUT}}$.

$$Slope = \frac{V_{OUT1} - V_{OUT2}}{P_{IN1} - V_{IN2}} \tag{22}$$

$$P_{INTERCEPT} = P_{IN1} - \frac{V_{OUT1}}{Slope} \tag{23}$$

$$P_{IN(UNKNOWN)} = \frac{V_{OUT(MEASURED)}}{Slope} + P_{INTERCEPT} \tag{24}$$

RF signals with power levels -5 dBm and 5 dBm from an AtlanTecRF low power signal generator were used for the calibration process. The obtained transfer function parameters are shown in Table 1.

Tab. 1. Calibration results

	Port 1	**Port 2**	**Port 3**	**Port 4**
$Slope$	-25.77	-25.52	-26.08	-25.59
$P_{INTERCEPT}$ [dBm]	31.40	31.67	32.47	30.82

As indicated in Equation 18, the S parameters of the proposed VNA itself is required to accurately measure the reflection coefficient of a load it is connected to. The S parameters were measured using the Agilent E5071c VNA with the C2W transitions in a setup like what is seen in Figure 18.

Fig. 18. Test set up for measuring coupling level for ports

Here, the Thru-Reflect-Line (TRL) calibration method was used to shift the Agilent VNA's measurement reference plane from the (coax) feed points to the two waveguide ports of the reflectometer. This essentially eliminated the effect of the C2W transitions and ensured proper characterization of the device-under-test (proposed VNA), which is key to its performance, particularly $\angle\Gamma_L$ measurements. The measured device parameters at 2.45 GHz were $S_{11} = -0.05666 - j0.01006$ and$S_{21} = -0.6875 - j0.5152$. These values were also store in the device's memory.

4.5. Power Handling Capability

The proposed VNA was designed to be used for high power applications. The device is expected to be used in a network fed by a 6-kW generator. Inspection of simulated E-field patterns showed that the maximum field strength, Emax in the VNA is approximately

61 kV/m for 6 kW (Figure 19). For an empty WR340 waveguide section sourced with 6 kW, Emax= 70 kV/m, giving a reference power handling capacity of 4 MW, at which arcing occurs. Thus, with an Emax of 61 kW, the VNA can operate safely at high power without the risk of arcing.

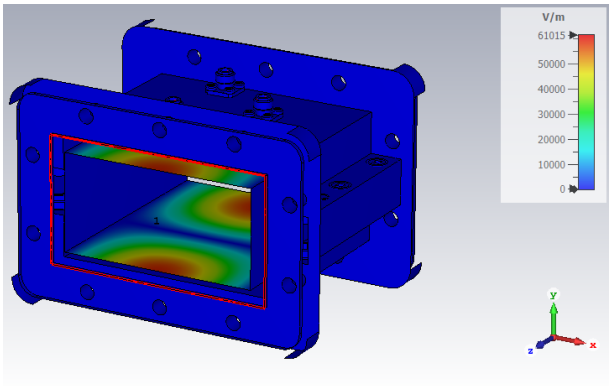

Fig. 19. Simulated E-field in the VNA when connected to a 6-kW generator running at 2.45 GHz

4.6. Evaluation

The performance of the proposed VNA was evaluated using the device to measure the reflection due to two different loads: a matched load and a terminated slide stub tuner. The experimental set-up comprised of the proposed VNA fed by a 13 dBm RF signal at 2.45 GHz with the loads connected on port 2. The experimental set-ups for measuring Γ_L of the matched and arbitrary loads using the developed VNA are shown in Figures 20 and 21 respectively. The reflection due to each of the two loads were also measured with the Agilent E5071c VNA and used as reference for comparison. The matched C2W transition presented a reflection coefficient with magnitude $|\Gamma_L|$=-23 dB and phase $\angle\Gamma_L$=145.3° when measured by the Agilent VNA (Figure 22) whereas the stub tuner load was configured such that it presented a $|\Gamma_L|$=-9.13 dB and $\angle\Gamma_L$=59.12° (Figure 23). Measurements using the proposed VNA produced $|\Gamma_L|$=-23.3 dB and $\angle\Gamma_L$=145.1° for the matched load whereas the recorded reflection due to the stub tuner load was $|\Gamma_L|$=-9.25 dB and $\angle\Gamma_L$=59.03°.

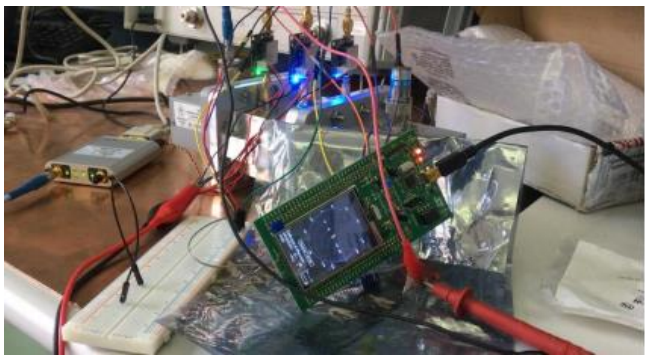

Fig. 20. VNA Evaluation Setup 1: Matched Load

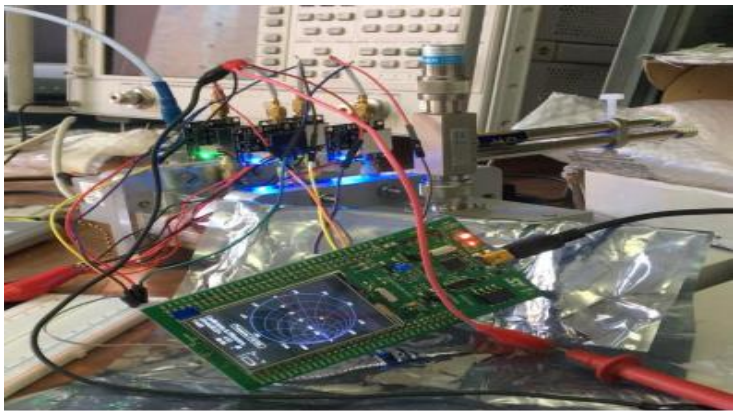

Fig. 21. VNA Evaluation Setup 2: Arbitrary Load

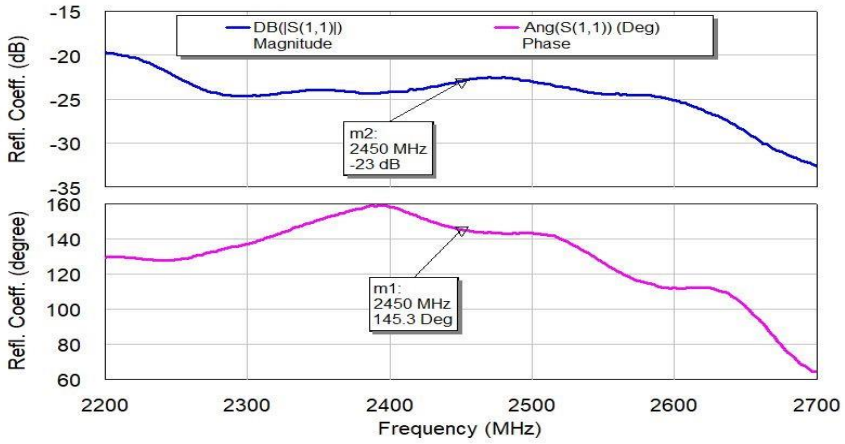

Fig. 22. Γ_L of the matched load measured the Agilent E5071c VNA

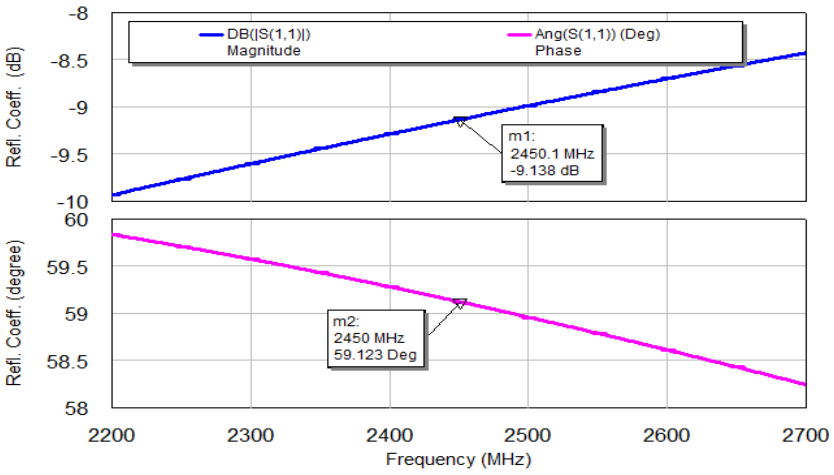

Fig. 23. Γ_L of the sliding tuner load measured the Agilent E5071c VNA

5. CONCLUSIONS

In this work, a compact vector network analyzer for high power microwave networks has been developed. The device was based on the six-port measurement technique where sampled powers from the network are used to derive the reflection coefficient at 2.45 GHz. The proposed analyzer is very useful in applications, which require online and inline parameter monitoring at multiple nodes in a microwave network, where employing commercial VNAs are not feasible in terms of cost, weight, safety, and complexity. Experimental results show a good and stable performance when compared to a commercial VNA, recording an average error of 0.21 dB and 0.15° error in complex reflection coefficient measurement.

Author Contributions

BK *– Idea, proposed design, and specifications and test and evaluation, read and approved final manuscript*

EOA *– Simulations and verification, read and approved final manuscript*

ETT *– Experimental set ups, tests, read and approved final manuscript*

ET – *Introduction, experimental strategies, read and approved final manuscript*

HNM *– Conclusion, experimental set ups, read and approved final manuscript*

BYA *– Related works, drawings, read and approved final manuscript*

Conflicts of Interest

The authors declare no conflict of interest.

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