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MULTI-CHANNEL DIGITAL-ANALOG SYSTEM BASED ON CURRENT-CURRENT CONVERTERS

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Abstract. An approach to building a multi-channel digital-analog system is proposed, in which, unlike the known ones, a code-current converter, a controlled current generator, and also a current communication block are used. For a given accuracy, this saves on the analog system equipment. It has been shown that the proposed principle of building a controlled current source in the form of a highly linear push-pull amplifier – current scalar on bipolar transistors with a grounded load – has a high output resistance and wide bandwidth, which allows the use of current switching to implement the multi-channel system mode.

Keywords: DAC, frequency response, phase response, linearity error of the transfer characteristic

WIELOKANALOWY SYSTEM CYFROWO-ANALOGOWY OPARTY NA PRZETWORNIKACH PRĄD-PRĄD

Streszczenie. Proponowane jest podejście do budowy wielokanałowego systemu cyfrowo - analogowego, w którym w odróżnieniu od znanego jednego przetwornika oferowany jest kod - prąd, generator prądu sterowanego, a także blok komunikacji prądów. Pozwala to zaoszczędzić na danej dokładności na sprzęcie analogowym systemu. Wykazano, że proponowana zasada budowy sterowanego generatora prądu w postaci wysoce liniowego wzmacniacza dwutaktowego – skaler prądu na tranzystorach bipolarnych z uziemionym obciążeniem ma wysoką rezystancję wyjściową i szerokie pasmo, co pozwala na zastosowanie przełączania prądu do realizacji trybu systemu wielokanałowego.

Słowa kluczowe: DAC, pasmo przenoszenia, przejście fazowe, błąd liniowości charakterystyki przenoszenia

Introduction

Many electronic systems [2, 6, 7, 11], such as programmable power supplies, signal distribution systems with a DAC in each information channel, multi-channel information transmission systems with sampling and storage devices with an analog multiplexer, use groups of digital-to-analog converters. At the same time, in some cases, it is advisable to use one DAC with multiplexer and output devices to capture or buffer the output signal. First of all, this refers to time distribution systems based on a single DAC with multiplexer and output devices for capturing or buffering the output signal.

It should be noted that in the case of using multiple DACs in the above systems, a number of important features need to be taken into account. First, each DAC has its own individual static errors and, if it is necessary to calibrate them, the system that implements this is complicated. Second, despite the ability to provide the required performance by the group DAC, it increases the power consumption and requires additional digital equipment.

On the other hand, the use of a single DAC requires an increase in its speed compared to the speed of any of the DACs in a group, as well as a high speed multi-channel output signal switch. A promising way to meet these requirements is the current principle in making these devices. Thus, the DAC must be made in the form of a code-current converter (CCC), the output buffer of the CCC is based on a controlled current generator (CCG), and a multi-channel analog switch is based on high-speed diode switches.

However, this approach is somewhat new, especially in the construction of CCGs, and it has not been sufficiently considered in the scientific and technical literature, so the topic of the article on the construction of a multi-channel digital-analog system on a single code-converter and controlled generator is urgent.

Research methods – providing increased speed of high-line multichannel code-analog conversion based on the current principle, in particular, using a controlled current generator.

1. Research objectives

The authors performed an assessment of the characteristics of various types of the equipment, in particular, their technical data, characteristic features, advantages and disadvantages:

1. to offer a generalized block diagram of a multichannel digital-analog system based on a single code-current converter and a controlled current generator;

2. to offer and analyze the principle of construction of a controlled current generator in the form of a highly linear push-pull amplifier – current scalar (PPACS) on bipolar transistors with a grounded load;
3. to estimate the static errors (zero offset and linearity) of the PPACS, as well as its speed, in particular the amplitude-frequency characteristic by computer simulation;
4. to consider the possibility of calibrating the error of the zero offset current ($I_{ZO,0}$) of the proposed multi-channel digital-analog system, by introducing corrections presented in digital form;
5. to provide practical recommendations for the practical implementation and application of the proposed multi-channel digital-analog system.

2. Solving research problems

Analyzing the purpose of the research, as well as the set of functions to be implemented, it is possible to heuristically synthesize the system as the block circuit shown in Figure 1. This circuit contains a code-current converter (CCC), controlled current generator (CCG), current switch unit (CSU), digital code adder (DCA), table of zero offset channel error correction codes, address bus (AB) of channel selection, set of output devices (SOD) to which currents I_1, I_2, \dots, I_k are supplied, and control block (CB), which ensures the functioning of the digital-analog system.

The system works in two modes. In the first mode, the zero offset errors of the source devices are determined. To do this, the DCA input receives zero codes ΔC_{in} and zero offset errors ΔC_0 .

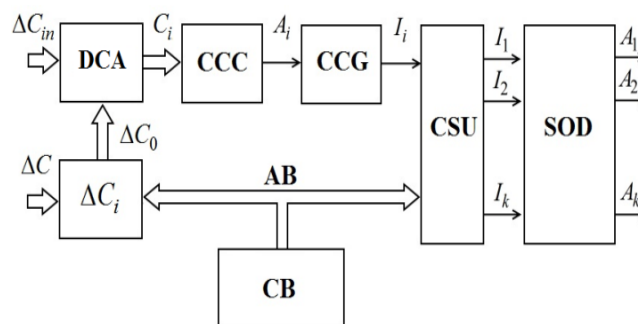


Fig. 1. Block circuit of a multi-channel digital-analog system with calibration $I_{ZO,0}$

Next the values of the zero offset errors $\Delta A_0, \Delta A_1, \dots, \Delta A_i$ are measured, the codes of which are sequentially entered in the table of corrections ΔC_i . The first mode is then completed and the system is ready to perform the main function. In the second mode, which is the main one, the work is done as follows. The i -th number of the required channel is selected by the CB command, and the converted code ΔC_{in} and the correction code ΔC_i are sent to the adder inputs. From the DCA output, the total code $C_i = C_{in} + \Delta C_i$ is sent to the CCC input and converted into a corresponding analog value A_i (current), the value of which is equal to:

$$I_i = \sum_0^{n-1} \alpha_i \cdot I_j,$$

where: $\alpha_i \in \{0;1\}$ is the binary bit coefficient C_i ; I_j is the value of the current of the j -th digit of the CCC, and n is the number of digits of the CCC.

The generated I_i is sent to the controlled current generator. It has the following requirements: high output resistance, as well as a wide bandwidth [9]. This is due to the specifics of the key current elements. Figure 2 shows a block circuit of the CCG and the current switch unit. Moreover, the first should be implemented in the form of a high-line push-pull DC amplifier (PPDCA), the schematic of which is considered in [1].

To ensure high output resistance R_{out} in the PPDCA, we have used negative feedback with the current removal method. During operation, the input current I_{in} is sent to the input push-pull cascade (InPPC) at the outputs of which we have branched components I' and I'' , which in turn are sent to the block of current gain and balancing (BCGB), where they are amplified and further branched into paraphase components I'_{out} , I''_{out} , \bar{I}'_{out} and \bar{I}''_{out} .

These components are sent to the direct and inverse inputs of the current reflectors CM1 and CM2. And the first outputs CM1 and CM2 combine to form the output bus (Out) of the circuit. At the same time, the second outputs CM1 and CM2 are connected to the inputs of the reflectors CM3 and CM4, the outputs of which are also integrated into the feedback bus (33).

Modes of cascades on a direct current (operating points) are set by generators of working currents I_p and mI_p .

Let us determine the low-signal current gain coefficient C_i when breaking the loop FB in the form:

$$C_i = \frac{I_{out}}{I_{in}}.$$

Let us assume that the PPDCA is built according to the scheme shown in Figure 2 [1]. Then it is easy to show that:

$$|I'| \approx |I''| = \frac{\beta_n \cdot \beta_p}{\beta_n + \beta_p},$$

where: β_n and β_p are low-signal current gain coefficient n-p-n and p-n-p of transistors, respectively.

Similarly, we have:

$$|I'_{out}| \approx |I''_{out}| \approx |\bar{I}'_{out}| \approx |\bar{I}''_{out}| = \frac{\beta_n \cdot \beta_p}{\beta_n + \beta_p}.$$

Taking into account the above, we finally get:

$$C_i = 2 \cdot \frac{\beta_n^2 \cdot \beta_p^2}{(\beta_n + \beta_p)^2}. \tag{1}$$

Substituting the values β_n and β_p in (1) for integrated transistors npn – NUHFARRY, pnp – PUHFARRY, we find the value C_i .

The feedback current I_{FB} is formed at the second output of the circuit. It is easy to show that when the loop FB breaks, the current transfer coefficient is $C_{i\ FB} \approx 2 \cdot C_i$.

Closing the circuit FB with resistors R_m (scale) and R_{\perp} , we obtain a controlled current generator, the transfer coefficient of which is equal to:

$$C_{ii} = \frac{C_{i\ fb}}{1 + \alpha C_{i\ fb}},$$

where: $\alpha = \frac{R_{\perp}}{R_m + R_{\perp}}$ is the transfer coefficient I_{FB} at the input of the circuit. Thus, taking into account that $\alpha C_{i\ fb} \gg 1$, we finally get:

$$C_{ii} = \frac{R_m + R_{\perp}}{R_{\perp}}. \tag{2}$$

It should be noted that expression (2) will be valid provided that $R_m \geq R_{in}$, where R_{in} is the input low signal resistance InPPC when the FB loop is broken. The low-signal value of this resistance is equal to the parallel connection of the input resistors InPPC from the elements T1 and T2 [1]. If $I_p = 1\text{ mA}$, then $R_{in} = 5\text{ k}\Omega$.

Thus, it is desirable that the condition $R_m \geq 5\text{ k}\Omega$ is met. The output low-signal resistance R_{out} of the CCG depends on both the output resistances R_{out1} and R_{out2} , and reflectors CM1 and CM2, respectively, and the depth FB, in particular, on the value of C_{ii} and C_i .

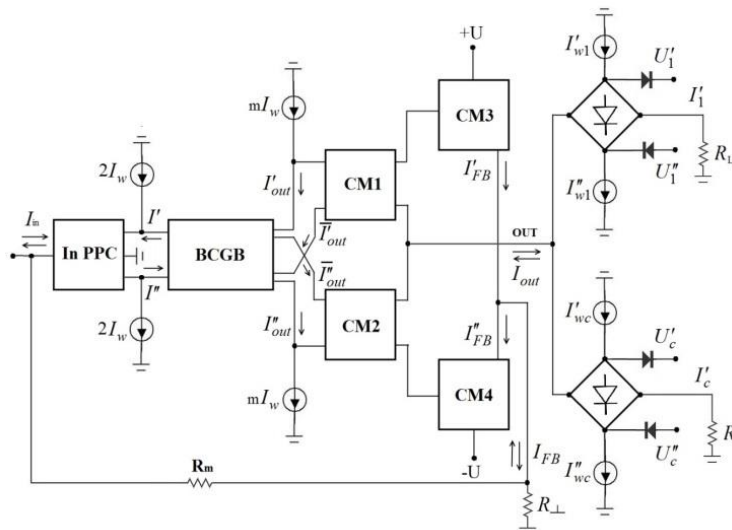


Fig. 2. Block circuit of PPDCA with current output and CSU

It is known from the theory of transistor amplifier circuits in the case of using a negative connection with current removal [10] that this leads to an increase in the output resistance. In our case, we have:

$$R_{out} = (R_{out1} \parallel R_{out2}) \cdot (1 + \alpha K_{I33}),$$

where: $R_{out1} \approx \frac{1}{2} \cdot R_{c\ n-p-n}$, $R_{out2} \approx \frac{1}{2} \cdot R_{c\ p-n-p}$ are the low-signal resistances of the collector junctions of the p-n-p and n-p-n transistors.

Taking into account that:

$$R_{out1} \parallel R_{out2} = \frac{1}{2} \cdot \frac{R_{c\ n-p-n} \cdot R_{c\ p-n-p}}{R_{c\ n-p-n} + R_{c\ p-n-p}},$$

We have:

$$R_{out} = \frac{1}{2} \cdot \frac{R_{c\ n-p-n} \cdot R_{c\ p-n-p}}{R_{c\ n-p-n} + R_{c\ p-n-p}} \cdot \left(1 + \frac{1}{C_{ii\ fb}} \cdot C_i\right), \quad (3)$$

Formula (3) is valid if the condition $R_m \gg R_{in}$ is met. If $*R_m$ is not high enough, then in (3), you need to substitute the coefficient:

$$\gamma_{FB} = \frac{R_m + R_{\perp}}{R_{in} + R_m + R_{\perp}},$$

It takes into account the loss of current transfer from the FB circuit to the PPDCA input. In the case of building a CCG on the above transistors and $I_p = 1\text{ mA}$, in mode $R_{in} = 0$, we have $1.4\text{ G}\Omega$.

If R_{in} changes in a certain range, then R_{out} changes due to the dependence of R_c on the current collector.

Computer simulation of the dependence $R_{out} = f(I_{out})$ allowed us to obtain a set of initial characteristics in the range $I_{in} = -100\ \mu\text{A} \div 100\ \mu\text{A}$, in particular for $C_{ii} = 10$, ($R_m = 2.0\text{ k}\Omega$, $R_{\perp} = 225\ \Omega$) as shown in Figure 3.

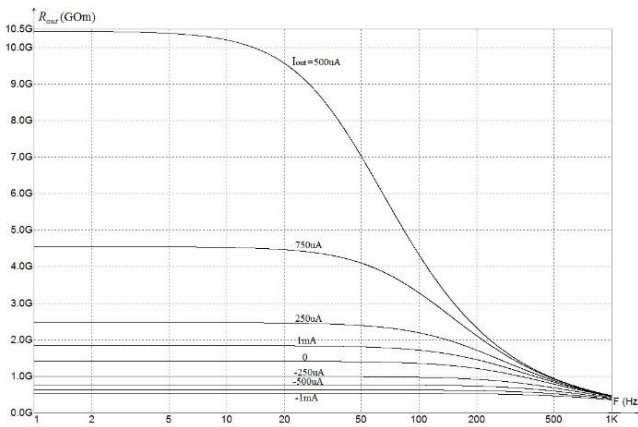


Fig. 3. Graphs of dependence $R_{out} = f(I_{out})$ in the frequency band at $C_{ii} = 10$

The graphs show that the output resistance decreases slightly when the direction I_{out} changes from direct to inverse.

The dependence R_{out} as well as the linearity errors on C_{ii} are given in the following table.

Table 1. Linearity errors and output resistance PPDCA

C_{ii}	2	5	10	20	100
R_{out} [M Ω]	406	688	1200	401	40
ΔI_{LIN} [nA]	0.98	1.4	2.1	42	2100
δI_{LIN} [%]	$0.98 \cdot 10^{-4}$	$1.4 \cdot 10^{-4}$	$2.1 \cdot 10^{-4}$	$42 \cdot 10^{-4}$	$21 \cdot 10^{-3}$

The change R_{out} is explained by the fact that in the range $I_{out} = -1\text{ mA} \div 1\text{ mA}$ at the outputs CM1 and CM2, the balance mode changes, during which there is a redistribution of collector currents between the p-n-p and n-p-n transistors, which have a significant difference between current gain β_n and β_p , and also different collector resistances.

The CCG output is connected to the bridge diode keys (BDK) of the current switch unit. The BDK operating points are set by operating current generators $I'_{w1}, I''_{w1}, I'_{w2}, I''_{w2}, \dots, I'_{wc}, I''_{wc}$, and control is carried out by digital signals (voltages) $U'_1, U''_1, U'_2, U''_2, \dots, U'_c, U''_c$, respectively. It should be noted that to ensure the functioning of the BDK, it is necessary that the values of operating currents I'_{wi} and I''_{wi} are slightly greater than I_{out} . If the levels I'_{wi} and I''_{wi} are at the level of milliamperes, then the BDK supports correspond to tens of ohms.

Under these conditions, the relative methodological error of the switching currents is equal to:

$$\delta I_{cm} = \frac{R_{BDK}}{R_{BDK} + R_{out}},$$

where: R_{out} is the output resistance of the CCG. If R_{out} has the meaning of hundreds of units of M Ω , then δI_m has is of the order $\sim 10^{-5} \div 10^{-4} \%$.

Of course, using the proposed principle of switching currents, this error can be ignored in most cases.

At the same time, due to the presence of the instrumental component of switching errors:

$$\delta I_{BDK} = \frac{|I'_{wi}| - |I''_{wi}|}{I_w},$$

As a result of the fundamental limitations on the exact fit of the levels I'_{wi} and I''_{wi} , this component must be taken into account in the form of corrections made in the form of codes ΔK in the table of corrections to the multi-channel code-analog system. For convenience of zero offset error $I_{ZO,0}$, the CCG and BDK should be summed and generated in the form of correction codes for the corresponding channel.

It should also be noted that the application of the principle of current amplification allows us to achieve the maximum speed of the CCG, which is determined by the cutoff frequencies of bipolar transistors. So the bandwidth of a single gain PPDCA when $R_L = 100\ \Omega$ reaches $\sim 1.6\text{ GHz}$. This can be seen from the amplitude-frequency characteristic of the device, the graph of which is shown in Figure 4.

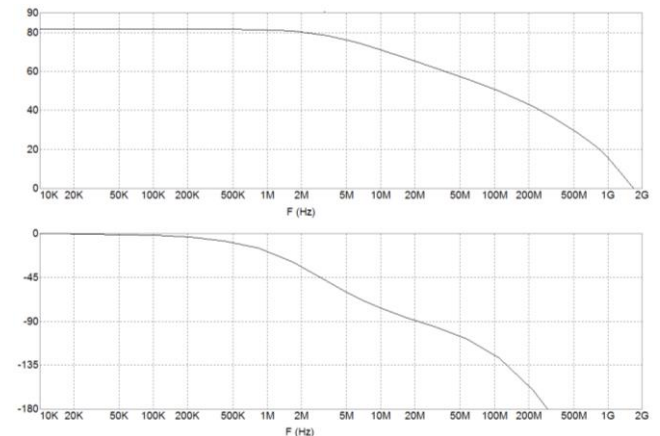


Fig. 4. Amplitude-frequency characteristic of PPDCA with a load of $100\ \Omega$

It is necessary to look at the recommendations for the use of types of output devices that are loads for the CCG and CSU, as well as this DA system. To maintain high speed and minimal linearity errors, it is desirable that the input supports R_{out} of the output devices are low; not more than hundreds of ohms. This is easy to achieve in current-voltage converters built on operational amplifiers, as well as sampling devices – storage of integrated type [3, 4, 5]. In some cases, the load can be the control winding of the stepper motor in the tracking code – the angle of rotation of the shaft [8].

3. Conclusions

- 1) An approach to building a multi-channel digital-analog system is proposed, in which, unlike the known ones, there is a code-current converter, a controlled current generator, and a current communication block. For a given accuracy, this saves on the analog system equipment.
- 2) The proposed principle of construction of a controlled current generator in the form of a highly linear push-pull amplifier – current scalar based on bipolar transistors with a grounded load has been analyzed. It has been shown that this device has a high output resistance and a wide bandwidth, which allows current switching to be used to implement a multi-channel system mode.
- 3) By computer simulation, the errors of zero offset $I_{ZO,0}$ and linearity have been analyzed and it has been proved that $I_{ZO,0}$ can be reduced by calibration by introducing corrections presented in digital form.
- 4) Practical recommendations and conditions of practical application of the considered multichannel DA system have been given for different types of output devices performing the role of a load.

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