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# DSTATCOM-BASED 15 LEVEL ASYMMETRICAL MULTILEVEL INVERTER FOR IMPROVING POWER QUALITY

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***Abstract.*** *This study suggests an asymmetric multilevel inverter based on DSTATCOM that employs SVPWM techniques to produce higher output levels. There are two steps in the suggested inverter. One full bridge and two half bridges make up the inverter's main stage. A full bridge converter had four switches and a single DC source, while half bridges have separate DC sources with a voltage ratio of 1:3:3. Every cell has a fixed neutral point and is connected in a cascaded fashion. The inverter's performance is not improved by setting the DC source values equally. A folded cascaded H-bridge circuit running at a line frequency makes up the second circuit. Control plan PWM's space vector modulation was used to verify the suggested topology. Each control scheme's specific methodology as well as switching pulses are covered in great detail. In MATLAB/Simulink, the suggested system has been simulated with an output voltage of 350 V and an output current of roughly 3.5 A.*

**Keywords**: DSTATCOM, THD reduction, PWM scheme, multicarrier PWM scheme, SVPWM scheme

## 15-POZIOMOWY ASYMETRYCZNY FALOWNIK WIELOPOZIOMOWY OPARTY NA TECHNOLOGII DSTATCOM POPRAWIAJĄCY JAKOŚĆ ZASILANIA

***Streszczenie.*** *W niniejszym opracowaniu zaproponowano asymetryczny falownik wielopoziomowy oparty na DSTATCOM, który wykorzystuje techniki SVPWM do wytwarzania wyższych poziomów wyjściowych. Proponowany falownik składa się z dwóch stopni. Jeden pełny mostek i dwa półmostki tworzą główny stopień falownika. Przetwornica z pełnym mostkiem ma cztery przełączniki i pojedyncze źródło prądu stałego, podczas gdy półmostki mają oddzielne źródła prądu stałego o stosunku napięć 1:3:3. Każde ogniwo ma stały punkt neutralny i jest połączone kaskadowo. Ustawienie jednakowych wartości źródeł prądu stałego nie poprawia wydajności falownika. Złożony kaskadowy obwód mostka H pracujący z częstotliwością sieciową tworzy drugi obwód. Do weryfikacji proponowanej topologii wykorzystano modulację wektora przestrzennego PWM. Szczegółowo omówiono metodologię każdego schematu sterowania, a także impulsy przełączające. W programie MATLAB/Simulink zasugerowany system został zasymulowany przy napięciu wyjściowym 350 V i prądzie wyjściowym około 3,5 A.*

**Słowa kluczowe**: DSTATCOM, redukcja THD, schemat PWM, schemat PWM z wieloma nośnymi, schemat SVPWM

## Introduction

"Multilevel voltage source inverters had a practical option for high-power Direct Current to Alternating Current conversion applications during the past few years" [11]. A Multilevel Converter (MLI) is an apparatus that creates a staircase waveform by connecting numerous input DC levels (from capacitors or DC sources) and power semiconductors. When compared to traditional inverters, the power switches in MLIs undergo less voltage stress [13]. Furthermore, the harmonic profile of the multilevel waveform is superior than that of the two-level waveform derived using traditional inverters. The reduction in voltage stress and the fault-tolerant operation are two added advantages of MLIs [14]. Additionally, scientists are investigating how to employ MLIs for less-power applications. By improving the levels improves the quality of the multilayer waveform [9]. On the other hand, it negatively impacts a lot of power semiconductor devices and related gate driver circuits. This tends to lower system efficiency and dependability while also increasing system complexity and cost. Therefore, in practical applications requires a fail in the power switches and gate driver circuits for a high resolution waveform. NPC, CHB and FC converters are the topologies for multilevel voltage output that have been thoroughly researched and made commercially accessible. However, with more output levels comes a increase in power switches, conducting at once, and the total cost of the system [6, 7]. As a result researchers are still concentrating on finding new ways to lower the number of components in multilevel topologies. These methods fall into three categories: using asymmetric sources with topological modifications, combining topological modifications with asymmetric source configurations. Here, a topology with alternating DC sources is devised. Furthermore, the suggested topology has resemblance to the CHB topology for symmetric input DC sources. Therefore, in renewable resources with a significant number of available isolated DC sources, the topology can serve as a utility interface [1, 3]. It can be applied to middle order voltage drive application, where separate battery sources are given by a phase shifting transformer with numerous secondary windings, which is typically utilized to reduce line current distortion [12, 15]. For the inverter, a control method based on SVPWM is provided along with simulation results. Furthermore, a comparative suggested topology and the current topology is provided [4, 8]. The final section discusses potential changes that could be made to this recently created MLI. The multilayer inverters' overall harmonic distortion of voltage. Research indicates that evaluating multilevel voltage quality might be challenging when dealing with numerically derived voltage THD values, which are susceptible to computation errors [4, 5]. The smooth hyperbolic voltage THD upper and lower bound approximations for closest synchronous switching 1-phase and 3-phase inverters are described here. They can be used realistically as good reference values and are valid for uniformly distributed level counts and arbitrary modulation indices. From that shown for a 3-phase star connected balanced load with isolated neutral and phase symmetrical modulation, line and phase voltage THD are nearly the same for multilevel inverter utilized [2, 10].

## 1. Design of DSTATCOM based multilevel

A D-STATCOM, a distributed static compensation device, uses a two-level voltage source converter (VSC) to convert a single DC voltage to three-phase AC outputs. It consist of a storage device & coupling transformer. The VSC and AC system are connected in parallel, as seen in Figure 1 [1]. It serves three main works:

1. Regulation of voltage and compensation of reactive power.
2. Power factor improvement.
3. The current's harmonics are eliminated.

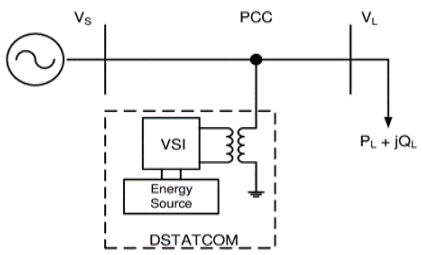


*Fig. 1. Schematic Diagram of a DSTATCOM*

## 2. Asymmetrical cascaded multilevel inverter

MLI describes a three-level DC source multilevel inverter here. The actual number of levels in this architecture is determined on how the DC sources are arranged. This innovative topology is used in my project to achieve the suggested MLI. Thus, fifteen output voltage levels are generated with this design. This topology significantly lowers the total number of devices for a given number of output levels [12].

### 2.1. Concept and topology

Due to their low THD output voltage wave shape and decreased voltage stress across power switches, MLIs are becoming more and more popular these days. On the other hand, the number of devices increases along with the level. Here we are providing a revolutionary topology to get maximum output level with a restricted no of elements. It can produce an output voltage waveform with 15 levels using this topology. In the voltage ratio of 1:3:3, is the necessary DC source. Two cascaded circuits are used in a single-phase hybrid multilevel topology to provide output voltages. The first circuit, dubbed the level creation circuit, consists of two diodes and six switches and is in charge of producing levels in positive polarity. Another circuit, known as the polarity generation circuit (marked cascaded circuit), consists of four switches and is in charge of determining the output voltage's polarity.

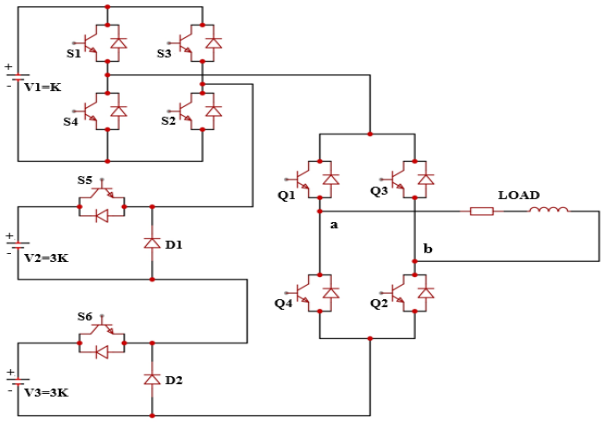


*Fig. 2. Proposed configuration for 1 phase fifteen level inverter*

A construction like this is seen in Figure 2 [10]. It is, in the conventional sense, a single-phase, 15-level inverter. The suggested inverter would be implemented with power switches like MOSFETs. To reach expected voltage level, this topology consists of 6+4 switches. The switches in the level generation circuit are $S_1$, $S_2$, $S_3$, $S_4$, $S_5$, and $S_6$, and the switches $Q_1$, $Q_2$, $Q_3$, and $Q_4$ are depicted in Figure 2. The ON/OFF switching procedure from 0 to 7k is displayed in Table 1.

Asymmetrical cascade MLI consist of 6 switches in level generation circuit having three DC source for each bridges, here it is designed with one H-bridge and two half bridge. In polarity generation circuit it consist of an H-bridge and load [4].

*Table 1. ON/OFF switching operation*

| State No. | VPN | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 2 | k | 1 | 1 | 0 | 0 | 0 | 0 |
| 3 | 2k | 0 | 0 | 1 | 1 | 1 | 0 |
| 4 | 3k | 1 | 0 | 1 | 0 | 1 | 0 |
| 5 | 4k | 1 | 1 | 0 | 0 | 0 | 1 |
| 6 | 5k | 0 | 0 | 1 | 1 | 1 | 1 |
| 7 | 6k | 1 | 0 | 1 | 0 | 1 | 1 |
| 8 | 7k | 1 | 1 | 0 | 0 | 1 | 1 |

### 2.2. Modes of operation

**Mode 1**

The output voltage $V_0$ = 0, where zero has 8th voltage level obtained by operating the device in mode 1. The diodes $D_1$ and $D_2$ as well as the switches $S_1$ and $S_3$ conduct in order to provide this output voltage. There is no current flow in this level; Figure 3 shows the current flow in mode-1 operation.

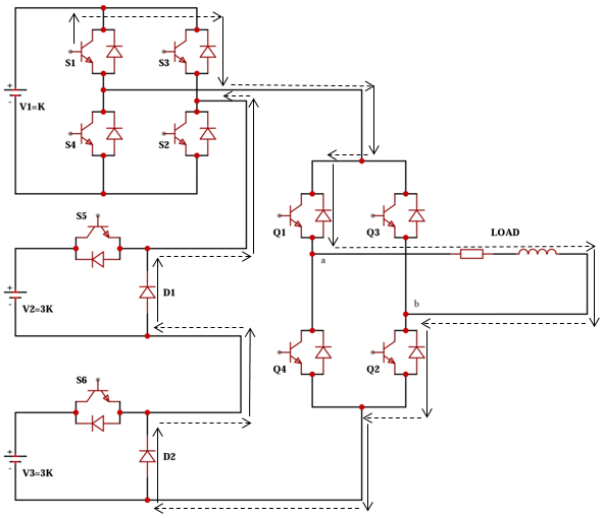


*Fig. 3. Circulation of current in Mode 1 operation*

**Mode 2**

The resultant voltage, $V_0 = V_1$, is obtained by using the fifteen level inverter in mode 2, where k is the seventh voltage level. The switches $S_1$ and $S_2$, as well as the diodes $D_1$ and $D_2$, conduct in order to provide this output voltage. The current flow in mode-2 operation is shown in Figure 4. Way of circulation path of the current flow is $+V_1$-$S_1$-$Q_1$-LOAD-$Q_2$-$D_1$-$D_2$-$S_2$-$V_1$

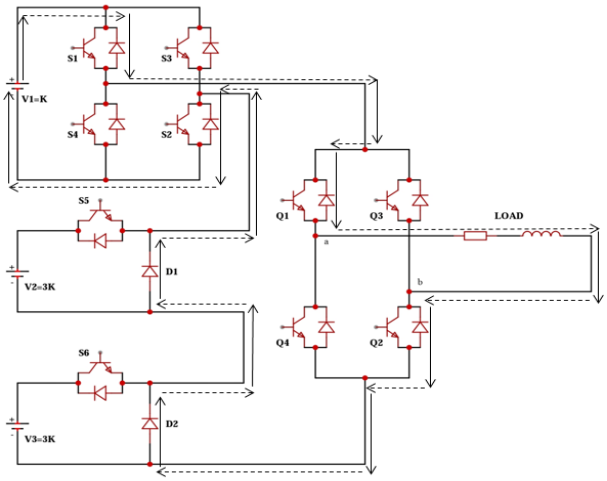


*Fig. 4. Current direction in Mode 2 operation*

**Mode 3**

The fifteen level inverter is operated in mode 3 to produce the output voltage, $V_0 = V_2 – V_1$, where the sixth voltage level is represented by 3k-k = 2k. This output voltage is created by conducting the switches $S_3$, $S_4$, $S_5$, and $D_2$. Figure 5 depicts the current flow for the mode-3 operation. The present flow pattern is as follows: LOAD-$Q_2$-$D_2$-$V_2$ – $+V_2$-$S_5$-$S_3$-$V_1$-$S_4$-$Q_1$.

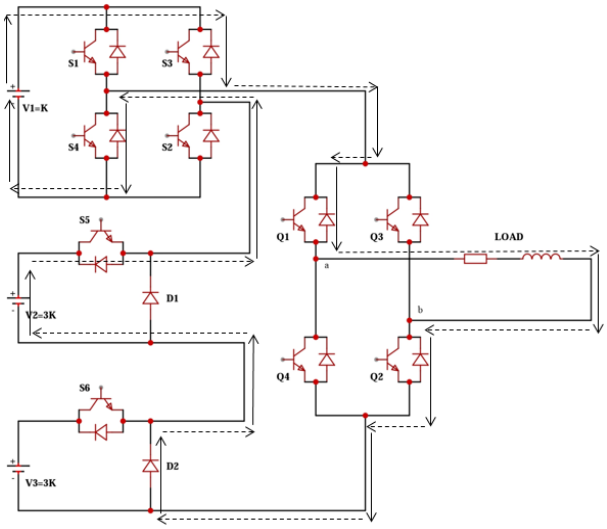


*Fig. 5. Flow of current in Mode 3 operation*

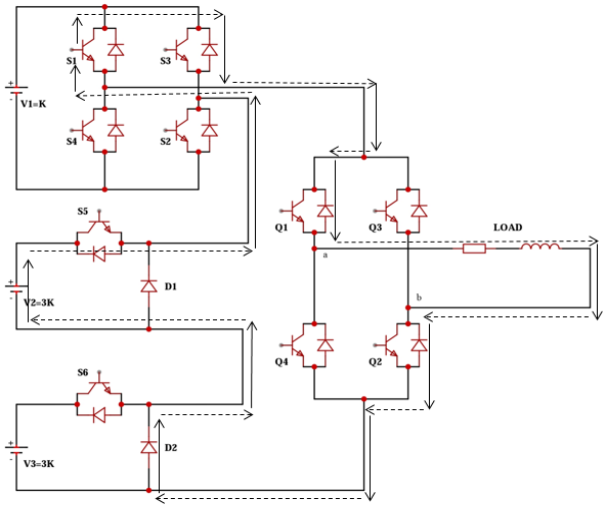


*Fig. 6. Current way in Mode 4 operation*

### Mode 4

Where output voltage $V_0 = V_2$, where 3k made as 5th output level, is obtained by operating the inverter in mode 4. This output voltage is obtained by conducting $D_2$ and the switches $S_1$, $S_3$, $S_5$, and $S_3$. The current flow in mode-4 operation is shown in Figure 6. The current flow's trajectory is such that $V_2$-$S_5$-$S_3$-$Q_1$-$S_1$-LOAD-$Q_2$-$D_2$-$V_2$.

### Mode 5

When $V_0 = V_2+V_1$, where 4k is the fourth voltage level of the 15 level inverter, is obtained by operating inverter in mode 5. This output voltage is obtained by conducting $D_2$ and the switches $S_1$, $S_2$, $S_6$, and $S_2$. The current flow in mode-5 operation is shown in Figure 7. The current flow's route is such -$S_6$-$S_1$-$V_2$-$Q_1$-LOAD-$Q_2$-$D_2$- and $V_3$.

### Mode 6

Where $V_0 = V_3+V_2-V_1$, where 5k as third level the third voltage level is obtained by using Mode 6 operation. To achieve this output voltage, conduct the switches $S_3$, $S_4$, $S_5$, and $S_6$. The current flow in mode-6 operation is shown in Figure 8. The current flow's trajectory is such that +$V_3$-$S_6$-$V_2$-$S_5$-$S_3$-$V_1$-$S_4$-$Q_1$-LOAD-$Q_2$-$V_3$.

### Mode 7

The output voltage $V_0 = V_2+V_3$, where 3k+3k=6k is the second voltage level is obtained by operating the inverter in mode 7. To achieve this output voltage, conduct the switches $S_1$, $S_3$, $S_5$, and $S_6$. The current flow in mode 7 operation is shown in Figure 9. The current flow's trajectory is such that +$V_3$-$S_6$-$V_2$-$S_5$-$S_3$-$V_1$-$S_4$-$Q_1$-LOAD-$Q_2$-$V_3$.

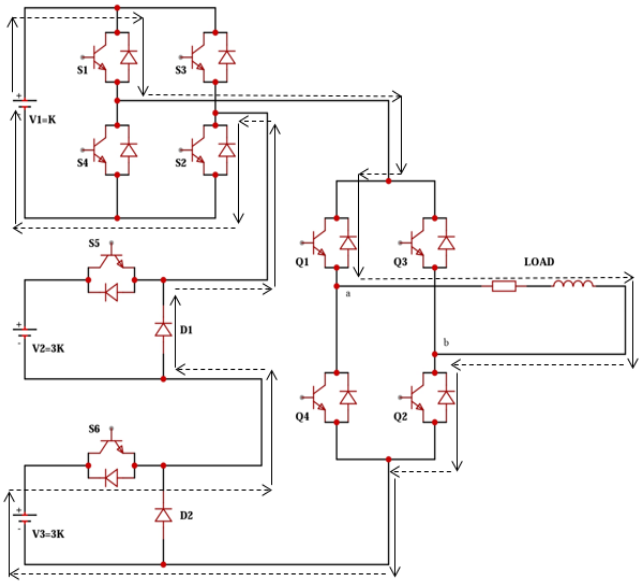


*Fig. 7. Current flow direction in Mode 5 operation*

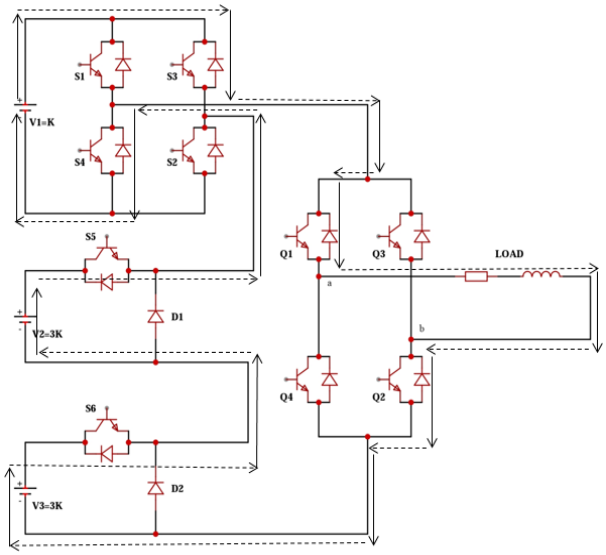


*Fig. 8. Mode 6 current path operation*

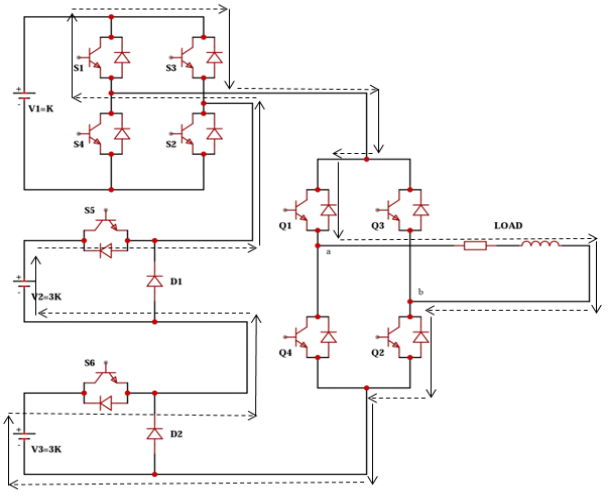


*Fig. 9. Current direction in Mode 7 operation*

### Mode 8

The output voltage $V_0 = V_1+V_2+V_3$ is obtained by operating the fifteen level inverter in mode 8, where the first voltage level is represented by the formula k+3k+3k=7k. To achieve this output voltage, conduct the switches $S_1$, $S_2$, $S_5$, and $S_6$. The current flow in mode-8 operation is shown in Figure 10. The way of the current direction is such that +$V_1$-$S_1$-$Q_1$-LOAD-$Q_2$-$V_3$-$S_6$-$V_2$-$S_5$-$S_2$-$V_1$.

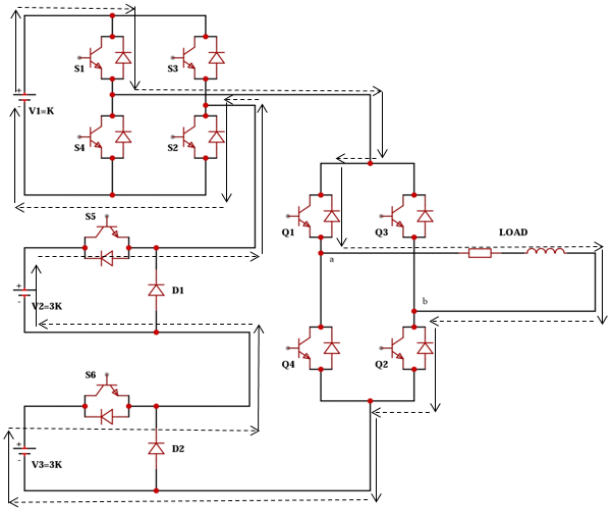


*Fig. 10. Current flow in Mode 8 operation*

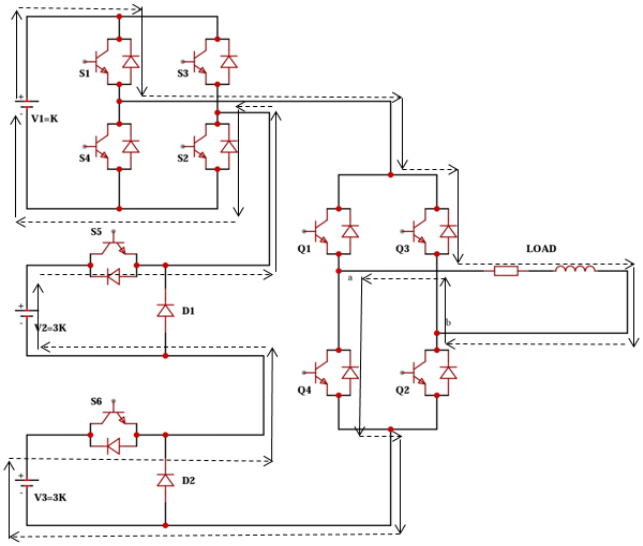


*Fig. 11. Current direction in Mode 9 operation*

**Mode 9**

By running the inverter in mode 9, one can achieve the output voltage $V_0 = V_1+V_2+V_3$, where -7k is the ninth voltage level of the fifteen level inverter. The switches $S_1$, $S_2$, $S_5$, and $S_6$ must be conducted in order to obtain this output voltage. Figure 11 displays the current flow in mode-9 operation. Current flow follows the following path: $+V_1$-$S_1$-$Q_3$-LOAD-$Q_4$-$V_3$-$S_6$-$V_2$-$S_5$-$S_2$-$V_1$.

**Mode 10**

Mode 10 operation is used to obtain output voltage $V_0 = V_2+V_3$ where -6k is the tenth voltage sequence of the fifteen level. In order to obtain this output voltage the switches $S_1$, $S_3$, $S_5$ and $S_6$ conducts. Figure 12 depicts the current flow in mode 10 operation. The path of the current flow is such $+V_3$-$S_6$-$V_2$-$S_5$-$S_3$-$S_1$-$Q_3$-LOAD-$Q_4$-$V_3$.

**Mode 11**

The output voltage $V_0 = V_3+V_2-V_1$, where -5k has eleventh voltage level of the 15 level inverter, is obtained by operating the inverter in mode 11. To achieve this output voltage, conduct the switches $S_3$, $S_4$, $S_5$, and $S_6$. The current flow in mode 11 operation is shown in Figure 13. $+V_3$-$S_6$-$V_2$+$V_2$-$S_5$-$S_3$+$V_1$-$V_1$-$S_4$-$Q_3$+LOAD-$Q_4$-$V_3$ is the current flow path.

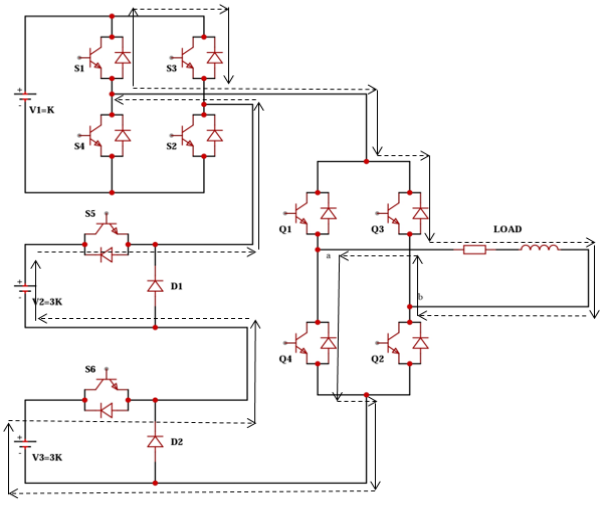


*Fig. 12.Current direction in Mode 10 operation*

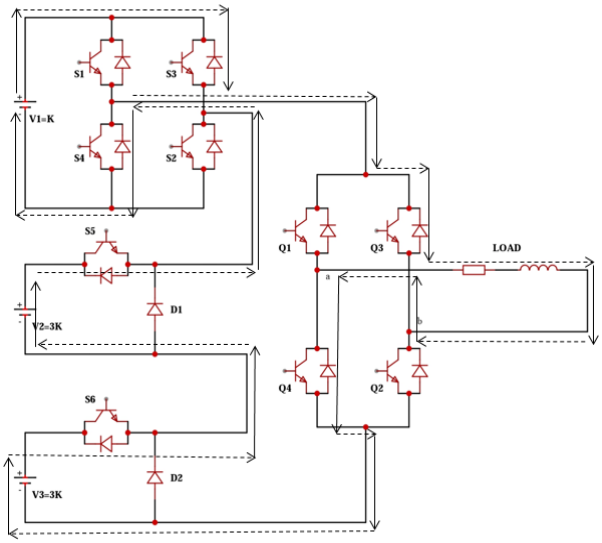


*Fig. 13. Current direction in Mode 11 operation*

**Mode 12**

The output voltage $V_0 = V_2+V_1$, where -4k as twelfth voltage sequence level obtained by operating inverter in mode 12. This output voltage is obtained by conducting $D_2$ and the switches $S_1$, $S_2$, $S_6$, and $S_2$. The current flow in mode 12 operation is shown in Figure 14. Current flow follows the following path: $+V_3$-$S_6$-$S_1$ $+V_1$-$V_1$-$S_2$-$Q_3$+LOAD-$Q_4$-$D_2$-$V_3$.

**Mode 13**

The final voltage $V_0 = V_2$ is obtained by operating the fifteen level inverter in mode 13, where -3k represents the 13th voltage level. This output voltage is obtained by conducting $D_2$ and the switches $S_1$, $S_3$, $S_5$, and $S_3$. The current flow in mode 13 operation is shown in Figure 15. The present flow path is as follows: $+V_2$-$S_5$-$S_3$-$S_1$-$Q_3$+LOAD-$Q_4$-$D_2$-$V_2$.

**Mode 14**

The output voltage $V_0 = V_2-V_1$, where -2k has fourteenth sequence of voltage in fifteen level inverter, is obtained by operating the inverter in mode 14. This output voltage is obtained by conducting $D_2$ and the switches $S_3$, $S_4$, and $S_5$. The current flow in mode-14 operation is shown in Figure 16. $+V_2$-$S_5$-$S_3$+$V_1$-$V_1$-$S_4$-$Q_3$+LOAD-$Q_4$-$D_2$-$V_2$ is the current flow channel.

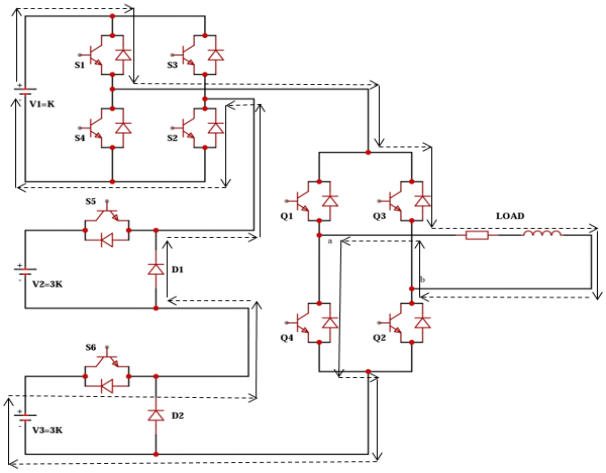


*Fig. 14. Current direction in Mode 12 operation*

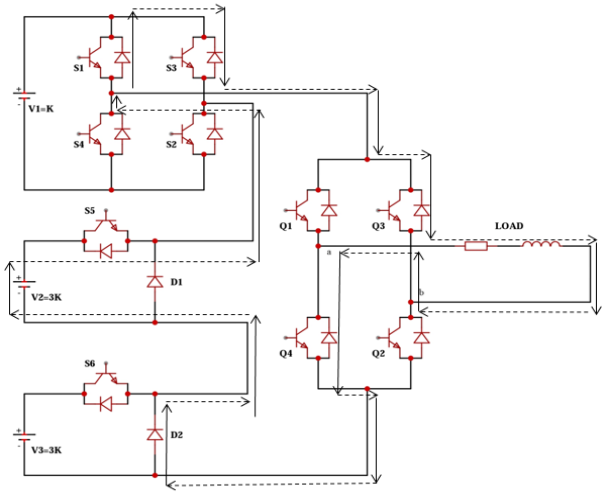


*Fig. 15. Current direction in Mode 13 operation*

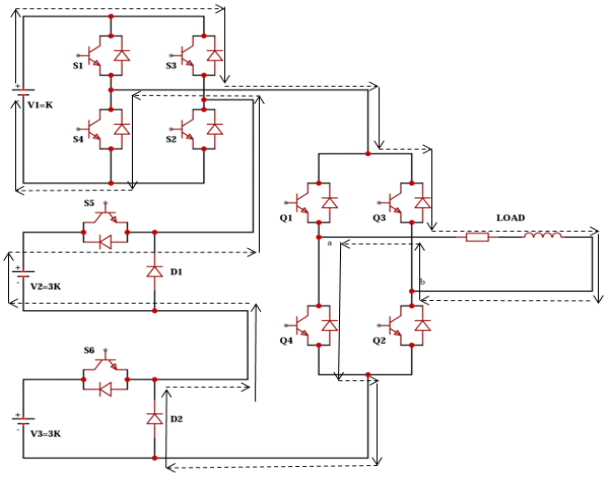


*Fig. 16. Current direction in Mode 14 operation*

**Mode 15**

The received voltage $V_0 = V_1$ is obtained by operating the fifteen level inverter in mode 15, where -k represents the fifteenth voltage level. The switches $S_1$ and $S_2$, as well as the diodes D1 and D2, conduct in order to provide this output voltage. The current flow in mode-15 operation is shown in Figure 17. Current flow follows the following path: $+V_1$-$S_1$-$Q_3$+LOAD-$Q_4$-$D_1$-$D_2$-$S_2$-$V_1$.

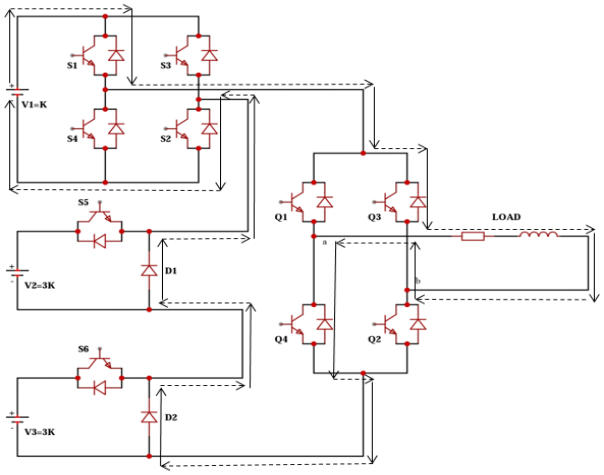


*Fig. 17. Current direction in Mode 15 operation*

## 3. Experimental analysis and simulation

### 3.1. Model of thirteen level inverter using SVPWM control scheme

To using a multicarrier PWM technique, the current multilayer inverter structure can be modified. Utilizing the MATLAB/Simulink tool, a block model of a 1-phase thirteen-level inverter is created to assess the effectiveness of the current topology with control scheme**.** There are three input DC sources that are used: $E_{dc1}$ = 40 V, $E_{dc2}$ = 80 V, and $E_{dc3}$ = 120 V. This simulation model includes a power circuit, a pulse generator, and a modulation control circuit. A voltage of around 240 V is generated by running the model. Figure 18 displays the 13 level inverter's entire simulation model.

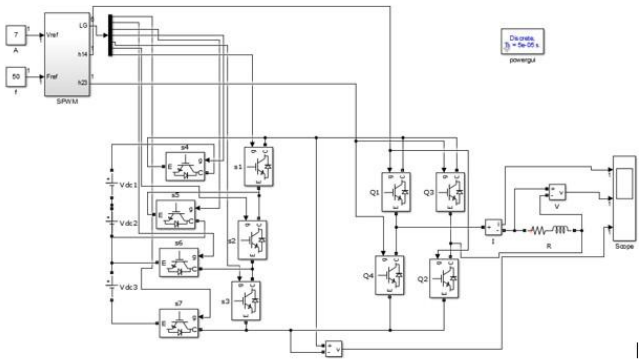


*Fig. 18. Overall Model of single 13 Level InverterModel of fifteen level inverter using SVPWM control scheme*

The control of the suggested structure is represented by a multi-carrier system with low switching frequency. The multi-carrier PWM method in a switching device determines each voltage level by comparing the carrier signal to a reference signal. However, the several switches in the suggested structure are not independent of each other. Therefore, in contrast to a two-level inverter, switching requires a suitable modulation. Figure 19 depicts the modulation control method [11–16]. The aggregated signal is produced by comparing the signals between carrier and sine wave. "In the output waveform, the aggregated signal "As" has the necessary number of levels. $C_1$, $C_2$, $C_3$, and $C_4$ are the carrier waveforms above the time axis, and $C_5$, $C_6$, $C_7$, and $C_8$ are the carrier waveforms below it". They are utilized to determine the k voltage value of the DC source and to produce the output voltage levels (0 to ±7k).

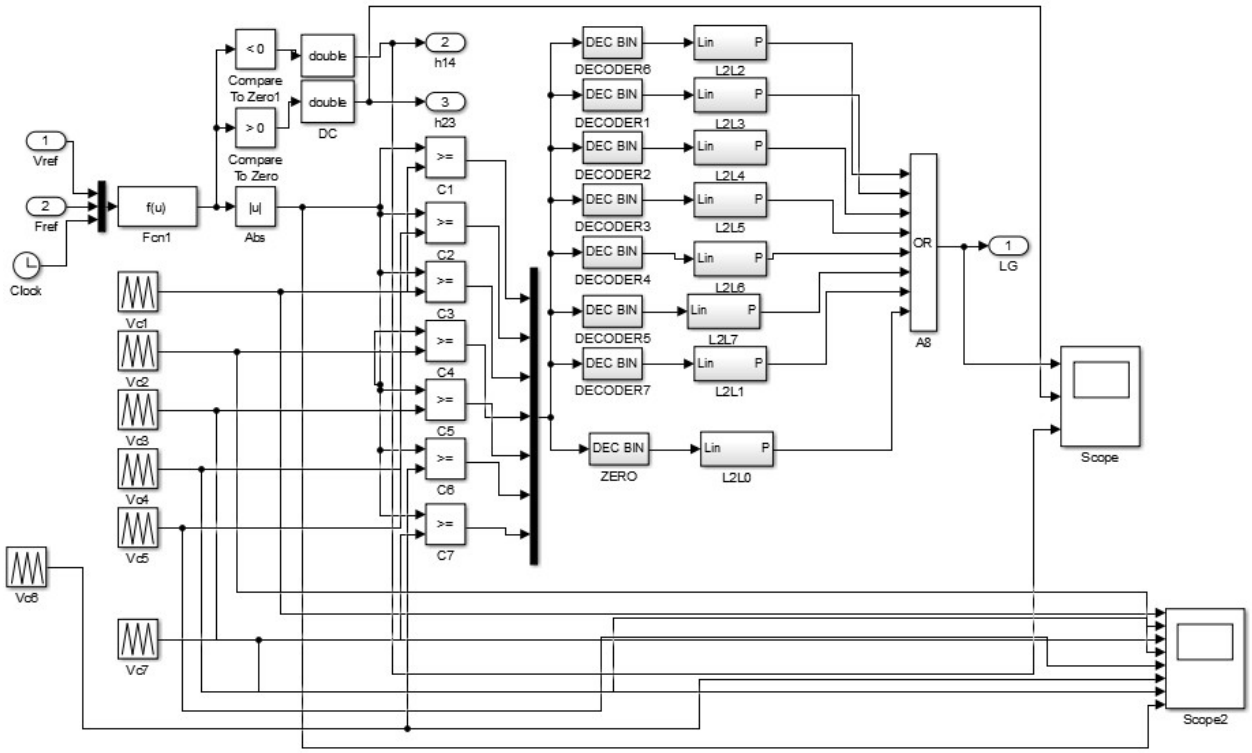


*Fig. 19. Generation of simulation model of suggested fifteen level inverter*

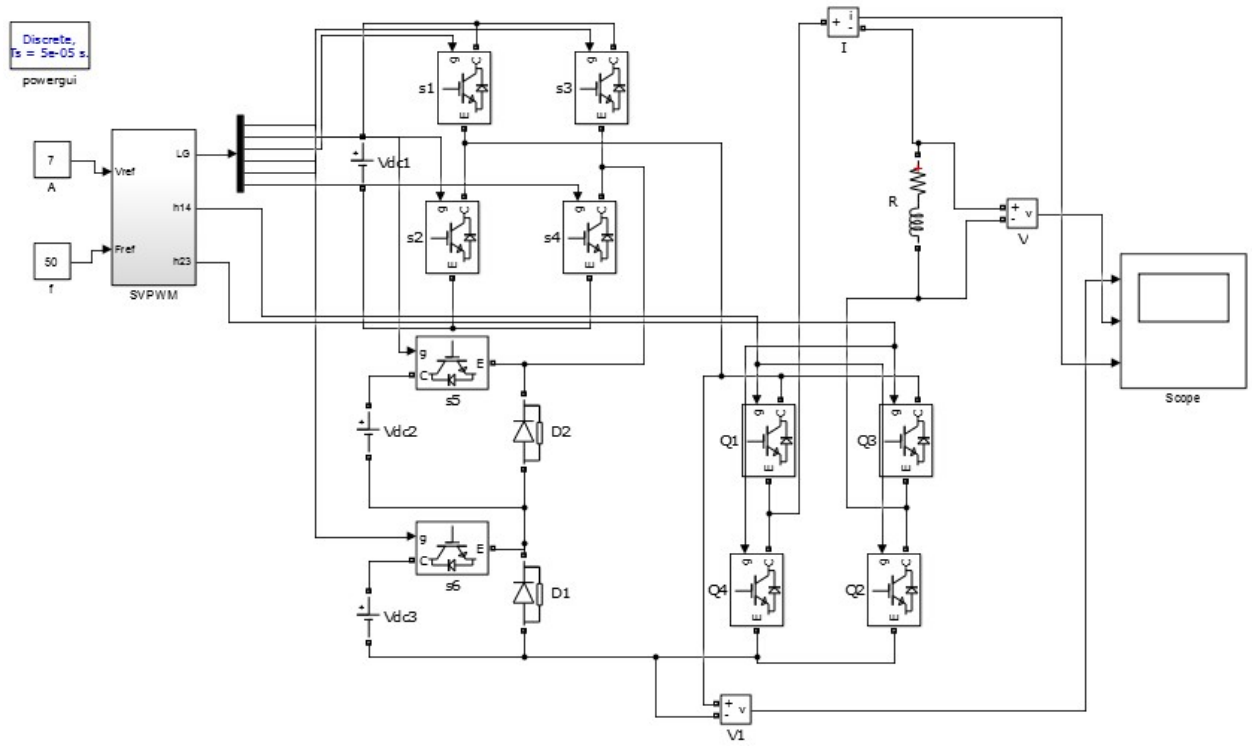


*Fig. 20. Simulation Model of Modified Fifteen Level Inverter*

The Figure 20 displays the MATLAB Simulink model of updated fifteen-level inverter, which includes the multilevel inverter that is being presented. The SVPWM method provides the gating signals for each switch. $V_1 = 50$ V, $V_2 = 150$ V, and $V_3 = 150$ V are the input voltages that are provided. Through model simulation, a voltage of ±350 V is produced [3, 12, 15].

Figure 21 depicts the hardware portion of the fifteen-level multilevel inverter. Power, driver circuit, and controller units are all included. Using a step down transformer, the AC input from the main supply is reduced in voltage. Through the use of a diode bridge rectifier, the stepped down AC voltage is transformed into DC voltage. The voltage can be maintained by connecting a voltage regulator to the DC output. Voltage regulators L7812cv and L7815 are employed in this instance. The controller unit uses the L7812cv regulator, whereas the driver circuit uses the L7815 regulator. To supply enough voltage to turn on the MOSFET switches in the multilayer inverter, a driver circuit is employed. The driver increases the microcontroller's voltage. Additionally, it has an optocoupler for isolation purposes, preventing MOSFET damage [6, 9].

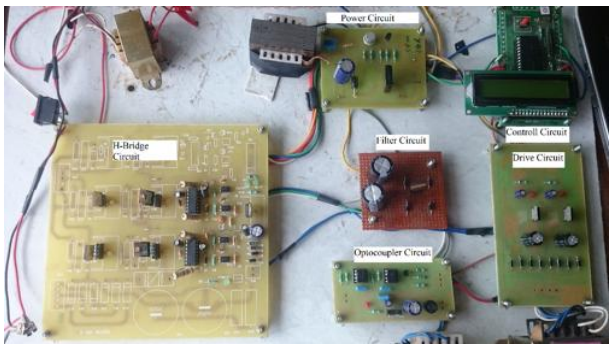


*Fig. 21. Hardware Section*

## 4. Result and discussions

### 4.1. Thirteen level inverter based on SPWM control scheme

Figure 22 displays the output waveforms for the 13-level inverter that is currently in use. This figure displays both the output voltage and the output voltage level that were produced from the multilayer inverter.

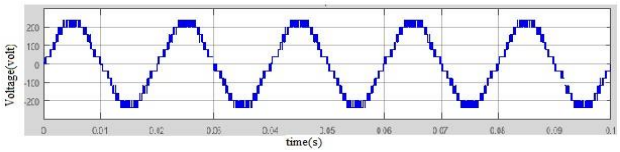


*Fig. 22. Thirteen level output*

Figures 23 and 24 display the THD for the output voltage and current, respectively, which are both approximately 28.74%. The input voltages are $S_1$ = 40V, $S_2$ = 80V, and $S_3$ = 120V, and the output voltage is ±240V in order to provide 13 levels at the output.

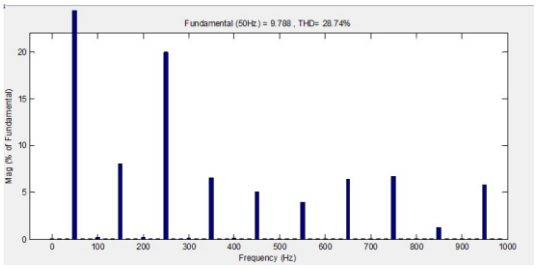


*Fig. 23. Output Voltage THD for 13 Level*

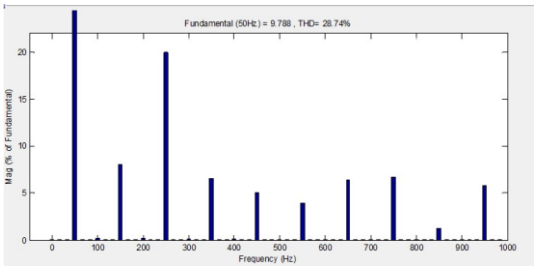


*Fig. 24. Output current THD for thirteen level*

### 4.2. 15 level inverter based on SVPWM control scheme

The waveform in Figure 25 depicts the output of the improved 15-level inverter.

Figures 26 and 27 display the THD for the output voltage and current, respectively, and are both approximately 10.83%. The input voltage is Vdc1 = 50V, Vdc2 = 150V, and Vdc3 = 150V to obtain 15 levels at output. The output voltage is ±350V [5].

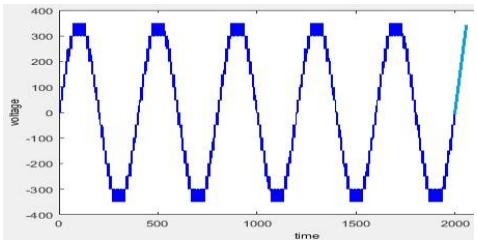


*Fig. 25. Proposed fifteen level output*

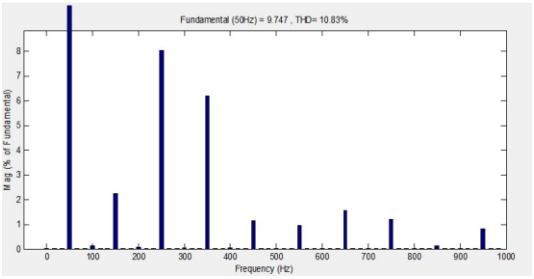


*Fig. 26. Output voltage THD for proposed fifteen level*

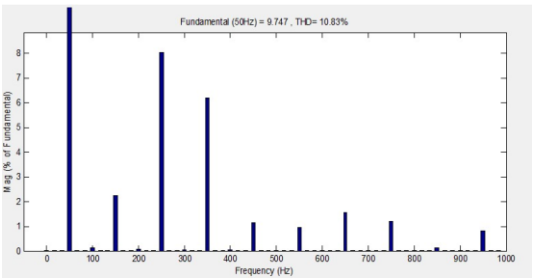


*Fig. 27. Output current THD for proposed fifteen level*

### 4.3. Comparison of existing and modified MLI

By Through a comparison of the output waveforms produced by the modeled systems, we can see that, in comparison to the current systems, the suggested system yields higher output voltage levels (15) and lower THDs (10.83%) with fewer components. Table 2 presents a comparison between the current and modified MLI [15].

*Table 2. Comparative analysis of different MLI*

| Different Parameters | Conventional MLI | Proposed MLI |
|---|---|---|
| Source input | E1=40V<br>E2=80V<br>E3=120V | E1=50V<br>E2=150V<br>E3=150V |
| Output voltage | ±240V | ±350V |
| Number of output level | 13 | 15 |
| Output voltage value of THD | 28.74% | 10.83% |
| THD for output current | 28.74% | 10.83% |
| Component count | 3dc Sources and 11 Switching Devices | 3dc Sources and 10 Switches |

## 5. Experimental results

The multilayer inverter circuit takes a 40 V or 80 V or 120 V battery source as its input. A digital storage oscilloscope was used to measure the signals from each terminal; the resulting waveforms are shown below. Figure 28 shows the pulse's output waveform that was generated for the switches, and Figure 29 shows the prototype with fifteen levels.

The improved fifteen-level MLI experimental setup with DSO, which produced the 15-level output across load resistor, as depicted in Figure 30. The controller board, driving circuit, and power circuit make up the experimental setup.

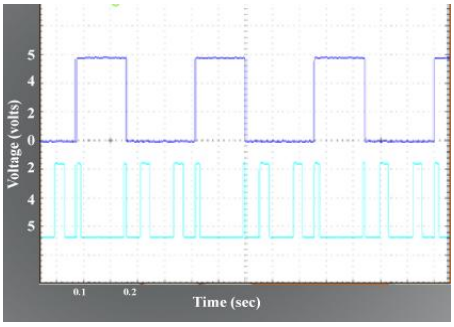


*Fig. 28. Generated pulses*

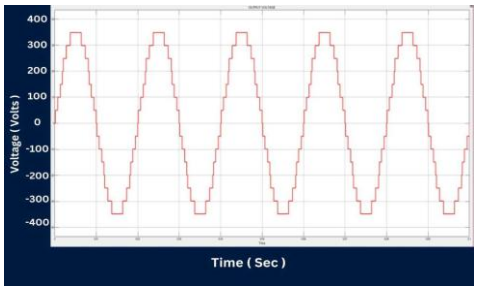


*Fig. 29. DSO output waveform of nine level inverter*


*Fig. 30. Prototype model of fifteen level*

With an input of 50 V, 150 V, and 150 V, the produced prototype yields an output voltage of ±350 V, or voltage level of fifteen. This developed prototype has fewer components and lower total harmonic distortions.

## 6. Conclusion

A fifteen-level Using MATLAB/Simulink, the simulation model for the suggested level multilevel inverter has been constructed and confirmed. To obtain maximum level of output, hence reduction in component count, since MLIs are becoming more and more popular. Numerous surveys of MLIs were carried out in support of this, and comparisons between various topologies were made using the results of those surveys. A unique multilevel inverter that uses the SVPWM technique can be built based on these surveys. Improve the reliability by putting this strategy into practice. The hardware prototype created and the hardware result was obtained with the suggested topology. At the end, a comparison between the multilevel inverters that are now in use and those that are being suggested is done. A hardware prototype was created using the suggested topology, and hardware outcomes were attained. Lastly, we will contrast the updated multi-level inverter with the multi-level inverter that is currently in place.

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