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PUSH-PULL VOLTAGE BUFFER WITH IMPROVED LOAD CAPACITY

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Abstract. *The article considers a method of increasing the load capacity of high-linear push-pull voltage buffer devices built on bipolar transistors. Buffer devices are designed to match the impedance of the signal generator to the impedance of the load and are essentially power amplifiers and act as an impedance converter with high input and low output impedances with a voltage transfer factor as close to unity as possible. The most common is the construction of buffer devices based on operational amplifiers with deep feedback in the voltage follower mode. At the present time, special attention is also drawn to push-pull circuits of buffer devices, which are considered in this article. An important characteristic of buffer devices is the load capacity, and to improve it (reduce the output resistance) of such buffer devices, a method based on the introduction of a push-pull DC output amplifier into the circuit is proposed. It is able to provide high linearity of the transmission characteristics and the required speed. New methods of structural and functional organization of the core of precision buffer devices with high and very high input resistance and the output push-pull current amplifier with different amplification factors are proposed. A schematic analysis of the static characteristics of the specified nodes, input resistance, load capacity and current amplification factor was performed. It has been proven that this method allows to significantly improve the load capacity of the voltage buffer.*

Keywords: schematic modeling, buffer, push-pull amplifier, bipolar transistors, load capacity

BUFOR NAPIĘCIA PUSH-PULL O ZWIĘKSZONEJ OBCIĄŻALNOŚCI

Streszczenie. *W artykule rozważono metodę zwiększenia obciążalności wysokoliniowych urządzeń buforujących napięcie typu push-pull zbudowanych na tranzystorach bipolarnych. Urządzenia buforowe są zaprojektowane tak, aby dopasować impedancję generatora sygnału do impedancji obciążenia i są zasadniczo wzmacniaczami mocy i działają jako konwerter impedancji o wysokiej impedancji wejściowej i niskiej impedancji wyjściowej ze współczynnikiem przenoszenia napięcia jak najbliżej jedności. Najbardziej powszechna jest konstrukcja urządzeń buforowych opartych na wzmacniaczach operacyjnych z głębokim sprzężeniem zwrotnym w trybie wtórnika napięciowego. Obecnie szczególną uwagę zwraca się również na obwody push-pull urządzeń buforowych, które są rozważane w tym artykule. Ważną cechą urządzeń buforowych jest obciążalność i aby ją poprawić (zmniejszyć rezystancję wyjściową) takich urządzeń buforowych, zaproponowano metodę opartą na wprowadzeniu wzmacniacza do obwodu wyjściowego push-pull DC. Jest on w stanie zapewnić wysoką liniowość charakterystyki transmisji i wymaganą prędkość. Zaproponowano nowe metody strukturalnej i funkcjonalnej organizacji rdzenia precyzyjnych urządzeń buforowych o wysokiej i bardzo wysokiej rezystancji wejściowej oraz wyjściowego wzmacniacza prądowego typu push-pull o różnych współczynnikach wzmocnienia. Przeprowadzono schematyczną analizę charakterystyk statycznych określonych węzłów, rezystancji wejściowej, obciążalności i współczynnika wzmocnienia prądu. Udowodniono, że metoda ta pozwala znacznie poprawić obciążalność bufora napięcia.*

Słowa kluczowe: schematyczne modelowanie, bufor, wzmacniacz push-pull, tranzystory bipolarne, obciążalność

Introduction

Buffer devices (BD) are analog units used in many electronic devices [4, 6, 7]. Buffer devices are designed to match the resistance of the signal generator with the load resistance and are essentially power amplifiers [4, 6, 16]. In this case, the voltage buffer acts as a resistance converter with high input and low output resistances with a coefficient of voltage transfer as close as possible to unity. It should also be noted that the dynamic and static characteristics of the mentioned buffers should not impair the metrological devices of which they are a part [2, 8, 9].

Many varieties of precision buffer devices are known, both in terms of circuit design and purpose. The most common is the construction of buffer devices based on operational amplifiers with deep feedback in the voltage follower mode [4, 6, 7]. Nowadays, special attention is drawn to push-pull circuits of buffer devices. It is proposed to use an approach for their construction, the essence of which is that the specified device is structurally divided into two parts. The first of which is a core in the form of a fast push-pull bipolar voltage buffer [1, 3]. The second part is a broadband push-pull DC amplifier whose output is connected to the load. They are able to provide high linearity of the transmission characteristic and the required speed of action [1–3]. At the same time, the material devoted to the analysis of buffer devices based on push-pull symmetrical structures is presented sporadically and unstructured in the scientific and technical literature. Therefore, the topic of the article, devoted to the construction of precision buffer devices based on push-pull symmetrical structures, is relevant [2, 10, 11].

1. The aim and objectives of the study

The purpose of the research is the analysis of the proposed methods of building highly linear buffers with increased load capacity, which differ from the known ones by being built on the basis of push-pull symmetrical structures, which makes it possible to improve their static and dynamic characteristics [12, 14, 15].

To achieve this objective, it is necessary to:

1. To propose and analyze new methods of structural and functional organization of precision buffer devices based on push-pull symmetrical structures.
2. Carry out a schematic analysis of the specified voltage static characteristics buffers, input resistance and load capacity [3, 13].
3. Carry out computer simulation of the considered schemes static characteristics of given voltage buffers, estimate the quantitative values of linearity errors of the transfer characteristic, input and output resistance, make a comparative analysis of the obtained results [5, 17, 18].

2. Methods

An approach to the construction of voltage buffers based on the use of current reflectors that function in a push-pull balanced mode, or on the basis of a slightly modified push-pull cascade is proposed [4, 6, 16]. The push-pull structure of voltage buffers provides the possibility of operation in the mode when the input (U_{in}) and output (U_{out}) voltages are bipolar, and the output current I_{out} can both flow in and flow out of the load. A simple scheme of such a device is shown in Fig. 1.

It is a bidirectional current reflector consisting of two current mirrors: on npn transistors T2 and T10, and on pnp transistors T5 and T13. Transistors T3 and T4 form the input stage and the input voltage source is connected to their bases. This design provides higher input resistance and lower zero offset current. To balance the operation of the circuit, an output stage on transistors T11 and T12 in diode connection is added. Collectors T3 and T4 are connected to negative and positive power sources, respectively, to ensure the constantness of their collector-base

voltages during operation of the circuit, transistors T8 and T7 serve, respectively. Current sources I1 and I2 set operating currents (equal to I_0) through transistors T1-T6. Transistors T1 and T9 balance the operation of transistors T2 and T10 by setting the base-collector voltage of transistor T2 equal to approximately $U_{be}(T1) \approx 0$ V of an open p-n junction. Transistors T6 and T10 perform a similar role for transistors T5 and T13 by setting the base-collector voltage of transistor T5 equal to approximately $U_{be}(T10) \approx 0$ V.

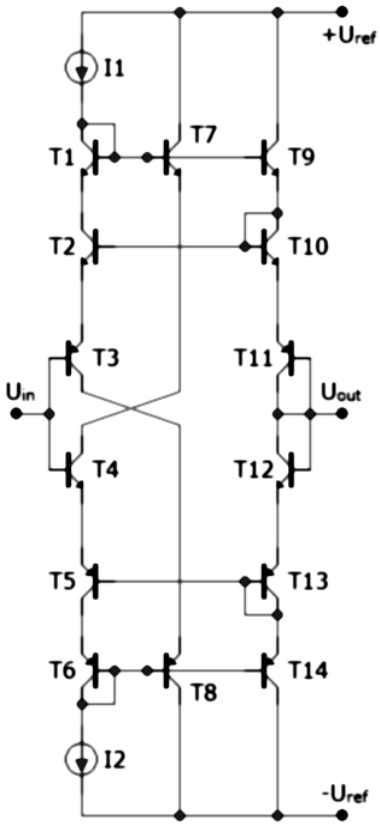


Fig. 1. Scheme of a simple voltage buffer

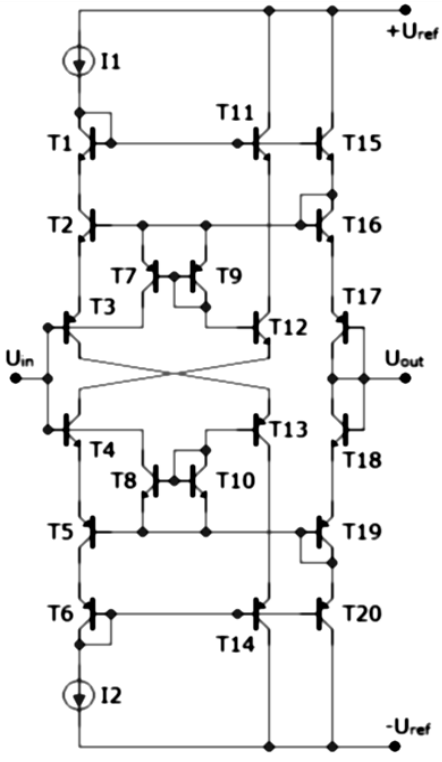


Fig. 2. Schematic of a voltage buffer with high input resistance

A more advanced scheme of such a device is shown in Fig. 2. Corrective circuits on transistors T7, T9, T12 and T8, T10, T13 are added to it. The current of the base of the transistor T12 is equal to the current of the base of the transistor T4 and with the help of a current mirror on the transistors T7, T9 is transmitted to the input of the circuit, but unlike the current of the base of T4, the current of the collector of T7 flows into the input of the circuit, similarly the current of the base of the transistor T13 is equal to the current of the base of the transistor T13 and with the help of a current mirror on transistors T8, T10 is transferred to the input of the circuit, but unlike the current of the base T3, the current of the collector of T8 flows from the input of the circuit. As a result, the input current of the circuit becomes almost zero, which significantly increases the input resistance of this circuit.

For the scheme in fig. 1, the following expression will be true:

$$U_{T2}^{be} + U_{T3}^{be} + U_{T4}^{be} + U_{T5}^{be} = U_{T10}^{be} + U_{T11}^{be} + U_{T12}^{be} + U_{T13}^{be} \quad (1)$$

If we assume that the output current is very small and neglect the base currents of the transistors, then the currents of the emitters of the transistors T10-T13 will be equal, we will denote them by I_0'. The emitter currents of transistors T2-T5 will be equal to I_0. Then taking in consideration the dependence $U = \varphi_T, ln(I/I_T)$ between current and voltage for a p-n junction, we get:

$$I_0 = I'_0 \quad (2)$$

Then the output voltage of the circuit will be equal to:

$$U_{out} = U_{in} + U_{T2}^{be} + U_{T3}^{be} - U_{T10}^{be} - U_{T11}^{be} \quad (3)$$

wherefrom

$$U_{out} = U_{in} \quad (4)$$

Thus, the circuit really works as a voltage follower (voltage buffer).

3. Experimental results

At small output currents, the input resistance of the circuit will be determined by he change in the base currents of transistors T7, T9 and T8, T14 when the collector-base voltage on them changes and, as a result, by the change in the operating currents of transistors T2-T5, the value of the input resistance will be:

$$R_{in} = \frac{1}{2} \cdot \frac{\beta_1 \cdot \beta_2 \cdot r_{k1} \cdot r_{k2}}{\beta_1 \cdot r_{k1} + \beta_2 \cdot r_{k2}} \quad (6)$$

where β_1, r_{k1} and β_2, r_{k2} are the current transfer coefficients of the base and the resistance of the collectors in the mode with the common base of the transistors T1 and T10, respectively. When substituting the parameters of the npn and pnp models of NUHFARRY PUHFARRY transistors [5] into this formula, the calculated value of R_{in} will be 45.4 MΩ, when simulating the one shown in Fig. 1 of the scheme in the Micro-Cap program we will get the value of R_{in} = 45.7 MΩ. When simulating the circuit in Fig. 2 in the Micro-Cap 11 program using npn and pnp transistor models NUHFARRY PUHFARRY [5], the values of input current – 317 nA, input resistance – 1 GΩ were obtained. Graphs of the dependence of the output resistance on the frequency for these schemes are presented in Fig. 3a, the output resistance is ≈ 30 Ω. The nonlinearity of the transfer characteristic of these circuits is ≈ 100 μV in the range from -5 V to +5 V, Fig. 3b.

With significant output currents, the input resistance of the circuit will be determined by the change in the base currents of transistors T9 and T14 when the output current flows through them, and as a result of the change in the operating currents of transistors T2-T5, the value of the input resistance will be:

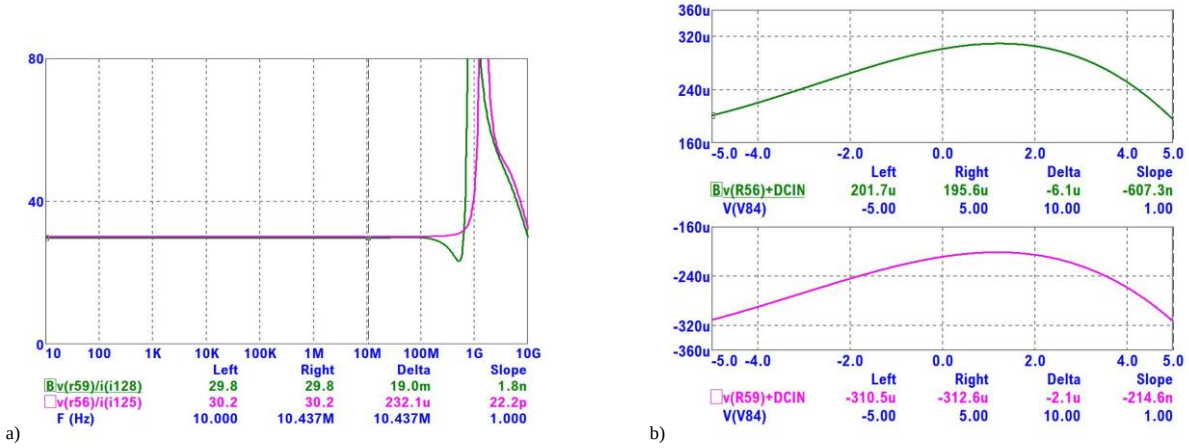
$$R_{in} = \beta_1 \cdot \beta_2 \cdot (R_{out} + R_l) \quad (7)$$

where R_l is the load resistance.

The output resistance of the circuit will be equal to:

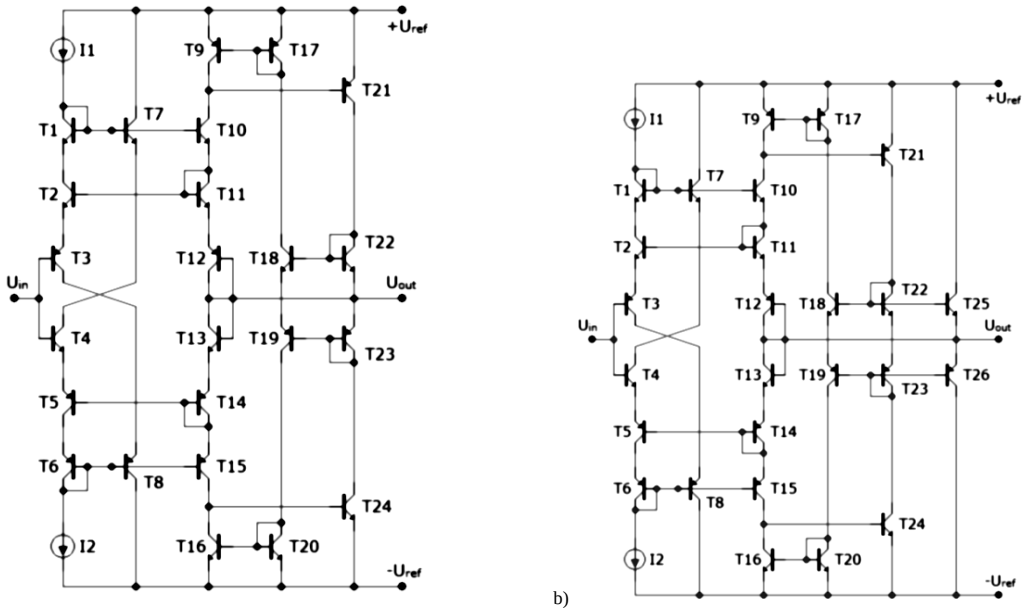
$$R_{out} = (r_{T10}^e + r_{T11}^e) \| (r_{T12}^e + r_{T13}^e) = r^e \quad (8)$$

where r_{Ti}^e is the differential resistance of the emitter junction of the i-th transistor.



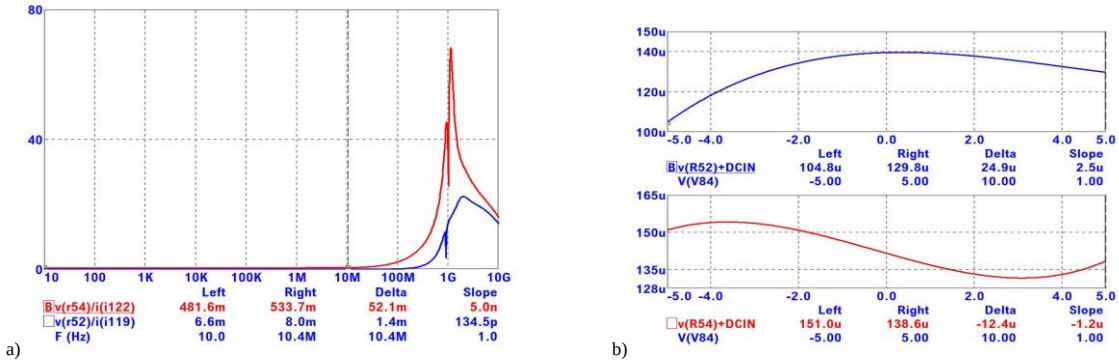
a) b)

Fig. 3. a) output resistance of BD; b) linearity of the transmission characteristic of the BD



a) b)

Fig. 4. Voltage buffers with low output resistance



a) b)

Fig. 5. a) output resistance of BD; b) linearity of the transmission characteristic of the BD

As you can see, the given circuit has a fairly high output resistance, and a significant output current reduces its input resistance. The scheme to compensate this weakness, shown in Fig. 4a.

It includes a push-pull voltage buffer and a push-pull amplifier stage on transistors T9, T16-T24. Current mirrors on transistors T9, T17 and T16, T20 serve to organize communication between the buffer and amplifying stages. Transistors T21, T24 amplify the differential components of the output current of the voltage buffer. Transistors T18, T19, T22, T23 form the output current generator. Its current output is the output of the circuit. Regarding the output current, the buffer splits it into two anti-phase components, which are then amplified by a push-pull amplifier stage and enter the output circuit of the circuit. At the same time, the output resistance is reduced by a factor of K_I, where K_I is the amplification factor of the cascades, and thus the majority of the output current flows through the push-pull amplifier stage of the output currents of the circuit.

$$K_i = \frac{1}{2} \cdot (\beta_1 + \beta_2) \tag{9}$$

To achieve an even lower output resistance, the circuit shown in Fig. 4b. Another amplification stage on transistors T25, T26 is added to it. At the same time, the output resistance also decreases by a factor of K_I, where K_I is the amplification factor of the cascades, which will be:

$$K_i = \frac{1}{4} \cdot (\beta_1 + \beta_2)^2 \quad (10)$$

When simulating circuit data in the Micro-Cap 11 program using npn and pnp transistor models NUHFARRY PUHFARRY [5], the following results were obtained.

Graphs of the dependence of the output resistance on the frequency for these schemes are presented in Fig. 5a, the output resistance is $\approx 0.5\,\Omega$ for the circuit in Fig. 4a, and $\approx 0.0066\,\Omega$ for the circuit in Fig. 4a. The nonlinearity of the transfer characteristic in the range from -5 V to +5 V is $\approx 34\,\mu V$ for the circuit in Fig. 4a, $\approx 2\,2\,\mu V$ for the circuit in Fig. 4b, Fig. 5b. As can be seen, significantly lower output resistance values and better linearity of the transfer characteristic were achieved.

4. Conclusions

1. It is shown that the proposed approach of structural and functional organization of precision buffer devices based on push-pull symmetrical structures allows to increase the load capacity and linearity of their transfer characteristics.
2. Mathematical models of the specified voltage buffers static characteristics, input and output resistance have been compiled. It is shown that the proposed approach allows significantly (by an order of magnitude or more) to reduce the linearity error and the output resistance.
3. Computer modeling of the voltage buffer of static characteristics of the considered circuits was carried out, the quantitative values of the linearity errors of the transfer characteristic and the output resistance were estimated, the results of which confirmed the reduction of the linearity error (by 3-5 times) and the output resistance (by 1-2 orders of magnitude).

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