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MODELLING OF SPINTRONIC DEVICES FOR APPLICATION IN RANDOM ACCESS MEMORY

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Abstract. *The article analyzes the physical processes that occur in spin-valve structures during recording process which occurs in high-speed magnetic memory devices. Considered are devices using magnetization of the ferromagnetic layer through transmitting magnetic moment by polarized spin (STT-MRAM). Basic equations are derived to model the information recording process in the model of symmetric binary channel. Because the error probability arises from the magnetization process, a model of the magnetization process is formed, which is derived from the Landau-Lifshitz-Gilbert equations under the assumption of a single-domain magnet. The choice of a single-domain model is due to the nanometer size of the flat magnetic layer. The developed method of modeling the recording process determines the dependence of such characteristics as the bit error probability and the rate of recording on two important technological characteristics of the recording process: the value of the current and its duration. The end result and the aim of the simulation is to determine the optimal values of the current and its duration at which the speed of the recording process is the highest for a given level of error probability. The numerical values of the transmission rate and error probability were obtained for a wide range of current values (10–1500 μA) and recording time of one bit (1–70 ns), and generally correctly describe the process of information transmission. The calculated data were compared with the technical characteristics of existing industrial devices and devices which are the object of the scientific research. The resulting model can be used to simulate devices using different values of recording currents: STT-MRAM series chips using low current values (500-100 μA), devices in the stage of technological design and using medium current values (100–500 μA) and devices that are the object of experimental scientific research and use high currents (500–1000 μA). The model can also be applied to simulate devices with different data rates, which have different requirements for both transmission speed and bit error probability. In this way, the model can be applied to both high-speed memory devices in computer systems and signal sensors, which are connected to sensor networks or connected to the IoT.*

Keywords: STT-MRAM, spin-polarized current, binary symmetric channel

MODELOWANIE URZĄDZEŃ SPINTRONICZNYCH DO ZASTOSOWANIA W PAMIĘCI O DOSTĘPIE SWOBODNYM RAM

Streszczenie. *W tym artykule analizowane są procesy fizyczne zachodzące w strukturach zaworów spinowych podczas procesu rejestrowania informacji, który występuje w urządzeniach z szybką pamięcią magnetyczną. Obiektem badań są urządzenia wykorzystujące magnetyzację warstwy ferromagnetycznej poprzez przenoszenie momentu magnetycznego za pomocą spolaryzowanego spinu (STT-MRAM). Wyprowadzono podstawowe równania potrzebne do modelowania procesu rejestrowania informacji w modelu symetrycznego kanału binarnego. W związku z tym, że prawdopodobieństwo błędu wynika z procesu magnesowania, stworzony jest model procesu magnesowania, który został wyprowadzony z równań Landaua-Lifshitza-Hilberta przy założeniu magnesu jednodomenowego. Wybór modelu jednodomenowego wynika z nanometrycznej wielkości płaskiej warstwy magnetycznej. Opracowana metoda modelowania procesu rejestrowania informacji określa zależność wskaźników, takich jak prawdopodobieństwo błędnego bitu i szybkość transmisji informacji, od dwóch ważnych właściwości procesu rejestrowania: natężenia prądu i czasu jego trwania. Końcowym rezultatem i zarazem celem symulacji jest określenie optymalnych wartości natężenia prądu i czasu trwania rejestracji informacji, przy których prędkość procesu zapisu będzie najwyższa dla danego stopnia prawdopodobieństwa błędu. Uzyskano wartości liczbowe dla szybkości transmisji i prawdopodobieństwa błędu dla szerokiego zakresu natężenia prądu (10–1500 μA) i czasu rejestracji jednego bitu (1–70 ns), które ogólnie poprawnie opisują proces transmisji informacji. Wyniki obliczeń zostały porównane ze specyfikacją techniczną istniejących urządzeń przemysłowych i urządzeń będących obiektami badań naukowych. Powstały model można wykorzystać do symulacji urządzeń wykorzystujących różne wartości natężenia prądu: układy szeregowe STT-MRAM wykorzystujące niskie natężenie prądu (500–100 μA), urządzenia na etapie projektowania technologicznego, które wykorzystują średnie natężenie prądu (100–500 μA) oraz urządzenia będące obiektami eksperymentalnych badań naukowych, które wykorzystują wysokie natężenie prądu (500–1000 μA). Model można również zastosować w symulacjach urządzeń o różnych szybkościach transmisji danych, które mają różne wymagania dotyczące zarówno szybkości transmisji, jak i prawdopodobieństwa błędu w jednym bicie informacji. W ten sposób model ten można wykorzystać zarówno w urządzeniach z szybką pamięcią w systemach komputerowych, jak i w czujnikach sygnałów, które są podłączone do sieci czujników lub podłączone do Internetu rzeczy.*

Słowa kluczowe: STT-MRAM, prąd spolaryzowany spinowo, symetryczny kanał binarny

Introduction

There are three development stages of the devices used for the processing of digital data, which use different states of magnetization and differ in physical mechanisms of magnetization reversal of active cells (MRAM). In the first generation of devices for magnetization reversal there is used the interaction with an external magnetic field. Devices of the second generation are based on the interaction mechanism of electron spins and magnetized layer with a small coercive force (STT-MRAM). STT-MRAM devices have two different topological implementations that differ in the direction of magnetization: perpendicular-to-plane and in-plane implementations [3]. To ensure two stable states, it is necessary that the thickness of the magnetic layer is much smaller than its transverse dimensions. Devices with parallel orientation have already been introduced into serial production of small memory modules with 64 Mb (2015) and 256 Mb (2016) [2]. Research is being conducted in the direction of constructing MRAM modules up to 4 GB [6].

STT-MRAM technologies are potentially attractive because they enable high-speed performance in the absence of device degradation (compared to FLASH modules) [2] and the refusal of uninterrupted power supply to memory chips (compared to SRAM modules). The theoretical basis for further speed increase of MRAM devices is that the transfer of the magnetization state of a magnetic field can occur much faster than the transport of charge carriers in classical semiconductor devices. This means that the switching time of the STT-MRAM can be further reduced. Therefore, according to the statements of some authors [3], in the future, magnetic memory devices will be able to conquer most of the RAM market.

The processes of magnetization reversal in STT-MRAM devices are of a statistical nature [9]. Therefore, methods of combating errors and the study of statistical patterns of their formation have great importance.

STT-MRAM devices are used in the embedded memory applications [10] for automotive industry [4] and the Internet [1, 8], which do not require the use of powerful computing systems. There are also studies on the use of these technologies in non-volatile operating computer memory, along with flash-memory technologies [7]. There are also projects in which MRAM devices are used for file systems [14].

In addition to that, STT-MRAM devices are used in the manufacture of relatively cheap authentication devices and the generation of secret keys [13], and the generation of cryptographic primitives (so-called software non-repetitive methods).

The ability of STT-MRAM devices to operate in the temperature range (-40°C to 125°C) [10] without the use of additional power sources makes it possible to use these devices in the IoT technologies and in sensor networks.

STT-MRAM devices are considered to be resistant to external interference. What is more, it is noted that there is a probability that there can occur the transition of the magnetization vector from one state to another. This is due to thermal fluctuations of the energy values of thermal fluctuations comparable with the values of the magnetization reversal energy. In [4], it is foretold that three types of errors may occur in STT-MRAM:

1) errors caused by higher values of current than technological standards;
2) errors caused by lower values of the recording current than technological standards;
3) errors caused by random magnetization.

The object of the study is a process of writing information in magnetic memory devices with a change in the state of magnetization of a free layer in a spin-valve, which is described by Landau-Lifshitz-Gilbert equation:

$$\frac{d\vec{M}}{dt} = -\gamma \cdot \left[\vec{M} \times \vec{H}_{eff}\right] - \frac{\alpha}{M_s} \cdot \left[\vec{M} \times \frac{d\vec{M}}{dt}\right] + \vec{T}_{s.t.} \quad (1)$$

or after simplification:

$$\frac{d\vec{M}}{dt} \approx -\gamma \cdot \left[\vec{M} \times \vec{H}_{eff}\right] - \frac{\alpha \cdot \gamma}{M_s} \cdot \left[\vec{M} \times \left[\vec{M} \times \vec{H}_{eff}\right]\right] + \vec{T}_{s.t.} \quad (2)$$

where $\vec{M}$ is a magnetization of a free layer; γ is is the gyromagnetic ratio; $\vec{H}_{eff}$ is a sum of all external magnetic fields; α is the phenomenological LLG damping constant; M_s is a saturation value of a free layer magnetization; $\vec{T}_{s.t.}$ is the moment of interaction between magnetic moment $\vec{M}$ and spin moment of the polarized current (s.t. – spin torque).

The investigation of information writing processes in memory devices is carried out on the basis of discrete channel models with a given bit error writing probability.

The object of the study is the dependence of the probability of magnetization flipping of ferromagnetic layer with two stable states of magnetization on the value of writing current and its duration.

The purpose of the work is to determine the optimum current value and its duration in the process of one–bit writing, at which the highest rate of information recording is observed at the smallest probability of a bit error.

1. Mathematical models of physical processes in spin-valves

Let's consider a model of flipping magnetization that occurs in the writing process and limits the speed of the device, since the read-out processes tend to have more stable characteristics. We simulate the operation of the STT-MRAM device, in which the magnetization vector is directed along the plane of the magnetic layer. The geometry of the device, as well as the direction of the electron flux, is shown in Fig. 1.

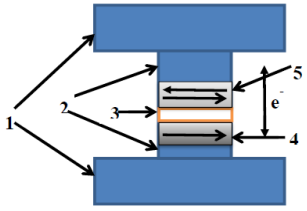

Fig. 1. Spin-valve structure: 1, 2 – contacts of a non-magnetic material, 3 – laye of a non-magnetic metal separating ferromagnets, 4 – ferromagnet with high coercive force (fixed layer), 5 – a ferromagnet with low coercive force (free layer, magnetic soft ferromagnet)

We construct a model of the error that occurs in the process of writing binary data. To do this, one must consider a device with STT-MRAM technology, in which the magnetization vector is directed along the plane of the magnetic layer. The geometry of the device as well as the direction of the electron flux is shown in Fig. 1.

The simulation of magnetization reversal in flat spin-valve structures with two possible stable states of magnetization is carried out on the basis of the LLG equation (macro-spin model) [11], which takes into account the interaction with the spin-polarized current $\vec{T}_{s.t.}$. The expression for the term $\vec{T}_{s.t.}$ in (2) has the following form [5]:

$$\vec{T}_{s.t.} = \left(\frac{I_S}{M_S^2}\right) \cdot \left[\vec{M} \times \left[\vec{M} \times \vec{n}_{ref}\right]\right] \quad (3)$$

The final form of the equation based on the macro-spin model that uses the amplitude value of the spin current, derived from the quantum-mechanical model of the electron flow, can be written as follows:

$$\frac{d\vec{M}}{dt} = -\gamma \cdot \left[\vec{M} \times \vec{H}_{eff}\right] - \frac{\alpha \cdot \gamma}{M_s} \cdot \left[\vec{M} \times \left[\vec{M} \times \left(\vec{H}_{eff} - \frac{I_s}{\alpha \cdot \gamma \cdot M_s} \cdot \vec{n}_{ref}\right)\right]\right] \quad (4)$$

where I_s is the spin current.

The mathematical model (4) of a single-domain magnet interacting with spin current allows us to establish the existence of two stable states of magnetization and to estimate the probability of transition from one state to another, depending on the value of write current. In the work, the probabilities of such flipping were determined for a wide range of values of write current.

Not taking into account the action of an external magnetic field in addition to the field of a fixed layer (the so-called field of anisotropy), the equation describing the precession of the magnetization vector of the free layer can be written as follows:

$$\frac{d\vec{M}}{dt} = -\gamma \cdot \left[\vec{M} \times \vec{H}_{eff}\right] - \frac{\beta \cdot \gamma}{M_s} \cdot \left[\vec{M} \times \left[\vec{M} \times \vec{n}_{ref}\right]\right] \quad (5)$$

where

$$\beta = \alpha - \frac{I_S}{\left|\vec{H}_{eff}\right| \cdot \gamma \cdot M_S} \quad (6)$$

The equation (5) in the form is a classical equation of LLG. Oppositely, however, the coefficient β can take both positive and negative values.

As can be seen in (6), the coefficient β changes the sign at a certain threshold value of the spin current. Given [5] that the spin current (7) is directly proportional to the usual current, it is possible to find the threshold value of the current below where no magnetization flipping occurs:

$$I_s = \hbar / 2e \cdot (I \cdot \eta) = (I \cdot \eta) \cdot 10^{-16} \; J / s^2 \quad (7)$$

where $\hbar$ is the Planck's constant; η is the spin polarization; e is the electron's charge.

The probability of returning the spin-valve to the previous state is determined by the following expression [5]:

$$p(\tau, I) = 1 - \exp\left\{-\frac{\pi^2 \cdot \xi}{4} \cdot \exp\left[-\frac{2\tau}{\tau_0} \cdot \left(\frac{I}{I_c} - 1\right)\right]\right\} \quad (8)$$

where τ is the time of a one-bit recording; I is a current; ξ is the ratio between the energy of thermal fluctuations and the energy barrier for magnetization reversal; τ_0 is the time constant; I_c is a value of the threshold current.

The model of the symmetric binary channel is used to determine the writing speed depending on the probability of error.

The capacity of the binary symmetric channel depends on the bit error and bit generation rate:

$$C = R \cdot \left[1 + p_e \cdot \log_2\left(p_e\right) + \left(1 - p_e\right) \cdot \log_2\left(1 - p_e\right)\right] \quad (9)$$

where C is a speed of recording, p_e is the bit error probability defined by expression (9), R is a bit rate.

Let's assume that the recording speed is the same as the capacity of channel C. What is more, we suppose that the generation rate of the bit stream depends inversely on proportion to the time of one-bit writing.

$$R = 1/\tau \quad (10)$$

where τ is a duration of one pulse.

2. Experiments

Let us consider in detail the physical values τ_0, I_c and ξ, which determine the probability of error of bit writing (9).

The parameter ξ is determined by the relation between the energy of the thermal vibrations which is $k_b \cdot T$ and the energetic barrier of the magnetization reversal in a one-domain approximation:

$$E_b = 1/2 \cdot M_S \cdot H_{eff}\,, \quad (11)$$

which is approximately $60 \cdot k_b \cdot T$ [11, 12].

Then, at room temperature (T = 300 K), the dimensionless multiplier for an exponent in equation (7) is equal to:

$$\frac{\pi^2 \cdot \xi}{4} = \frac{\pi^2}{4} \cdot 60 \approx 148 \quad (12)$$

In the absence of the action of an external magnetic field, the threshold value of the current, at which the conversion process is possible, is determined by the Gilbert damping constant α, the energetic barrier E_b, and the degree of spin polarization η [11]:

$$I_c = \left(2e/\hbar\right) \cdot \left(\alpha/\eta\right) \cdot E_b \quad (13)$$

We consider the value of the degree of current polarization to be 0.5.

Consequently, the value of the critical current is:

$$I_c = \frac{2 \cdot 1.9 \cdot 10^{-19}}{6.62 \cdot 10^{-34}} \cdot \frac{0.1}{0.5} \cdot 2.5 \cdot 10^{-19} \approx 22\mu A \quad (14)$$

Constant τ_0, which has the dimension of time, characterizes the return frequency of the magnetization vector to its previous state and is determined by the following relation [11]:

$$\tau_0 = \left(m_e/\mu_B\right)/\eta \cdot \left(I_s/e\right) \approx 8ns \quad (15)$$

where m_e is the mass of the electron; μ_B is the Bohr magneton, I_s is a spin current.

Then the dependence of the probability of the bit error writing on the current and its duration will be of the following form:

$$p\left(\tau, I\right) = 1 - \exp\left\{-148 \cdot \exp\left[-\frac{\tau}{4} \cdot \left(\frac{I}{22} - 1\right)\right]\right\} \quad (16)$$

Expressions (8) and (16) are basic for mathematical model of the writing digital information process in STT-MRAM. We have investigated the capacity of a channel and bit error probability for current values in the range of 50–200 μA and the time of a single bit writing in the range of 1–70 ns. It should be noted that the read current is 1–5 μA, which is due to another physical mechanism for reading based on the dependence of the logic gate resistance on the direction of current flow.

3. Results

The research was carried out for low (50–90 μA), medium (100–500 μA) and high values of write currents (500–1500 μA).

At low current values, the value of recording speed is 80 Mbps, and the optimum duration value of a one-bit writing varies from 25 ns (for a write current of 50 μA) to 13 ns (for a write current of 90 μA). For average currents, the maximum recording speed was 500 Mbps, and the optimal duration of a one bit ranged from 9 ns (for 100 μA) to 1.8 ns (for 500 μA). The high value of write currents makes it possible to achieve write speeds up to 1 Tbit/s, for currents of 1000 μA with the duration of a one bit of 1.1 ns. For a current of 600 μA, the speed is almost twice as low – 600 Mbps.

Table 1 summarizes the result of the one-bit duration simulation, the recording speed and the one-bit error probability at different current values requirements, and the bit error level and the recording speed.

The investigated range of current values was 50–1500 μA, covering various areas of possible application of the model, what are the devices of industrial production, design developments and experimental researches.

Table 1. Optimal values of simulated parameters

Modes	Write current, μA	The requirement for the highest recording speed			The requirement for equality of bit error probability to 10^{-4}		The requirement for the lowest error probability		
		Duration of a single bit writing, ns	The recording speed, Tb/s	The bit error probability	Duration of a single bit writing, ns	The recording speed, Tb/s	Duration of a single bit writing, ns	The bit error probability	The recording speed, Tb/s
Low current (industrial devices)	50	27.8–29.4	0.0307	0.0211–0.0127	37.6	0.0263	65	$1.5 \cdot 10^{-7}$	0.0154
	60	20.6–21.4	0.0417	0.0201–0.0143	32.8–33	0.0304	65	$9.6 \cdot 10^{-11}$	0.0154
	70	16.4–16.8	0.0527	0.0191–0.0154	26–26.2	0.0384–0.0381	65	$5.9 \cdot 10^{-14}$	0.0154
	80	13.8	0.0637	0.0165	21.4	0.0467	63	$1.1 \cdot 10^{-16}$	0.0157–0.016
	90	11.8	0.0747	0.0161	18.2–18.4	0.0549	53.6–54.8	$1.1 \cdot 10^{-16}$	0.0184–0.0187
Average current (research work with expected implementation)	100	10.2–10.4	0.0856	0.0146–0.0174	16	0.0624	46.6–47.6	$1.1 \cdot 10^{-16}$	0.0209–0.0224
	200	4.4–4.6	0.1951	0.0134–0.02	7	0.1426	20.6–20.8	$1.1 \cdot 10^{-16}$	0.0481–0.0485
	300	2.8	0.3045	0.0211	4.4	0.2268	13.3	$1.1 \cdot 10^{-16}$	0.0746–0.0758
	400	2	0.4101	0.0271	3.2	0.3118	9.8	$1.1 \cdot 10^{-16}$	0.1
	500	1.6	0.521	0.0246	2.6	0.384	7.8	$1.1 \cdot 10^{-16}$	0.1282
High current (experimental and scientific research)	600	1.4	0.6344	0.0149	2.2	0.454	6.4	$1.1 \cdot 10^{-16}$	0.1562
	800	1.1	0.8519	0.0212	1.6	0.624	4.6	$3.3 \cdot 10^{-16}$	0.2174
	1000	1.1	0.9774	0.0022	1.1	0.8307	3.8	$1.1 \cdot 10^{-16}$	0.2632
	1200	1.1	0.9969	$2.3 \cdot 10^{-4}$	1.1	0.9969	3	$5.6 \cdot 10^{-16}$	0.3333
	1400	1.1	0.9996	$2.3 \cdot 10^{-5}$	–	–	2.6	$3.3 \cdot 10^{-16}$	0.3846

4. Conclusions

The important problem of modeling the information recording speed based on the model of error of magnetization flipping in STT-MRAM devices is solved.

The scientific novelty of obtained results is a combination of the probability model of error in the process of magnetization reversal, based on the fundamental theory, and the binary channel model. Based on the model, the recording speed of information in STT-MRAM devices was studied in a wide range of write current values.

The practical significance of the model developed is that it enables a prediction of the probability of error of a single bit writing depending on the value of write current and its duration. the model also allows to determine the value of the write current and its duration at the permissible values of the probability of single bit writing.

A prospect for further research is an improvement of the bit error model, taking into account the asymmetry of the binary transmission channel.

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